Comparative assessment of III-V heterostructure and silicon underlap double gate MOSFETs

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Comparative assessment of III-V heterostructure and silicon underlap DG-MOSFETs, is done using 2D Sentaurus TCAD simulation. III-V heterostructure device has narrow-band $In_{0.53}Ga_{0.47}As$ and wide-band InP layers for body, and high-K gate dielectric. Density gradient model is used for simulation and interface traps are considered. Benchmarking of simulation results show that III-V device provides higher on current, lesser delay, lower energy-delay product and lower DIBL than silicon device. However III-V device has higher SS and lower I_{on}/I_{off} than silicon device. The results indicate that there is a need to optimize the I_{on}/I_{off}, SS and DIBL values for specific circuits.

1. Introduction

As MOSFETs are scaled to sub 20 nm dimensions, it becomes very difficult to maintain the necessary device performance, due to significantly increased short channel effects. Presently the device drive current is increased for rapid switching, at lower supply voltage. This leads to an exponentially increasing leakage current, causing excessive standby power dissipation [1]. There is a need to investigate new channel materials and improved device structures that would present us with energy efficient solutions at high switching speeds. High mobility III-V semiconductors have significant transport advantage, and are being extensively researched as channel materials for upcoming highly scaled devices [2–5]. But, majority of these III-V materials have considerably smaller bandgap as compared to silicon, leading to excessive band-to-band tunnelling (BTBT) leakage currents, which eventually limits their scalability beyond 22 nm technology node [1]. Thus there is need to find alternatives to overcome these leakages with some novel device structures and materials.

Double gate (DG) fully depleted MOS (DG MOS) devices provide excellent immunity to short-channel effect (SCE) and better scalability [6]. With the arrival of quasi-planar structures, like underlap DG MOSFET, fabrication of the double gate structures has become more feasible [6]. These underlap devices can substantially reduce short-channel effects, but degrades the drive current due to increase in effective channel length with underlap. HEMT (high electron mobility transistor) devices on the other hand, provide high ON state current (drain current $I_d = I_{d\,sat}$ and $V_{gs} = V_{ds(saturation)}$ and ultrafast performance due to III-V material on the channel, however, their OFF state control ($V_{gs} = 0$), gate leakage and scalability needs to be controlled [7].

Intend of this work, is to arrive at a new solution that takes into account both high performance and low leakage, but remains in the quasi-MOS regime which makes it achievable to fabricate the device without wide deviation from the existing technology. The new III-V heterostructure underlap device is aimed to achieve high ON state current requirement using bulk conduction arising from HEMT-like mechanism, and good OFF state control by DG MOSFET-like mechanism [7].

Followed by the description of the device and its operation in Sec. 2, we discuss the device simulation results and comparison in Sec. 3. Standard benchmarking techniques are used to evaluate the device performance.

2. Device description and operation

We simulate two different underlap DG MOSFET devices having gate length $L_g = 18$ nm, with an undoped ultra thin body (UTB). The device 1 channel consists of silicon with body thickness of 6 nm. The channel of device 2 (Fig. 1), consists of III-V heterostructure consisting of narrow-band $In_{0.53}Ga_{0.47}As$ layer of 4 nm region and two wide-band InP (t_2) layers of 1 nm each. The simulated device structure has source/drain regions doped at 10^{20} cm^3 and uses abrupt doping at source/drain ends. The source/drain lengths are 5 nm, the top and bottom gate has equivalent oxide thickness of $t_{ox} = 1.2$ nm. Device 1 uses SiO_2 (silicon dioxide) and device 2 uses high dielectric constant HfO_2 (hafnium dioxide) to minimize leakages. In both devices we assume symmetric underlap from gate to source and gate to drain sides.

Physical properties of narrow-band-gap $In_{0.53}Ga_{0.47}As$ materials and wide-band-gap InP materials are listed in the Table. $In_{0.53}Ga_{0.47}As$ having excellent electron mobility for narrow-band-gap layer and lattice matched InP for wide-band-gap layer are selected here. Narrow-band-gap material is sandwiched between the two wide-band-gap barrier layers and the channel is confined at the heterostructure interface. The barrier layer used has the conduction band edge offset with the channel and is nearly lattice matched with the

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Physical properties of $In_{0.53}Ga_{0.47}$ and InP

Material	E_g, eV	CBO, eV	VBO, eV	ε_0	Lattice constant, Å	μ_e, $cm^2/(V \cdot s)$	μ_h, $cm^2/(V \cdot s)$
InP	1.344	–	–	12.5	5.867	5400	200
$In_{0.53}Ga_{0.47}As$	0.74	0.22	0.38	13.9	5.868	12000	300

narrow-band layer to minimize the traps at its interface with the channel [8]. The III-V barrier layers provides:

(i) carrier confinement in the quantum well and

(ii) minimizes junction leakage and MOSFETs off state leakage current I_{off} [9].

As III-V semiconductor have high mobility and they will posses high injection velocities, which can increase the ON current with reduction in device delay. However due to this high mobility, the leakage current will also be high. To minimize the leakage high-K dielectric such as HfO_2 is used in device 2. III-V material has smaller transport mass, which gives higher injection velocity, however they have a low density of states (DOS) in the Γ-valley, resulting in reduced inversion charge (Q_{inv}) and consequently reduced drive current [1]. Also III-V materials inherently give rise to higher band-to-band tunnelling (BTBT) leakage current in comparison with Si [1]. High permittivity of these materials makes them more susceptible to short channel effects (SCE). Quantum confinement in ultrathin body plays a major role in reducing the BTBT leakage [1]. Lower density of state (DOS) resulting in reduced effective gate capacitance, and subsequently reduced inversion charge for a given gate voltage. By virtue of smaller transport effective mass m^*, III-V material based devices posses higher injection velocity (V_{inj}). Even though III-V materials have low Q_{inv}, due to higher injection velocity V_{inj}, they deliver higher drive current than silicon.

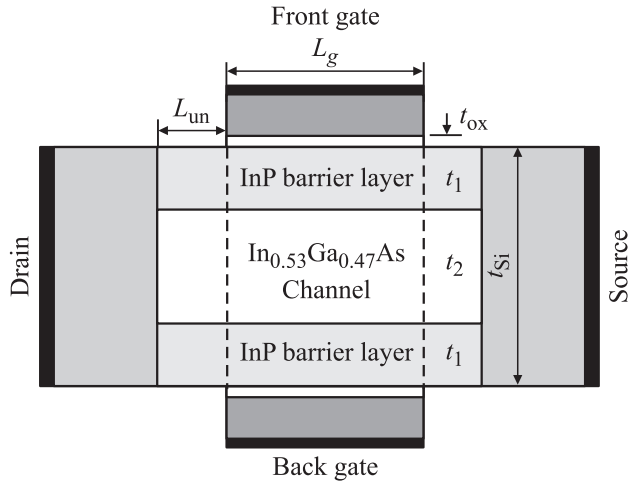

Figure 1. III-V heterostructure underlap DG MOSFET showing the source/drain side underlap (L_{un}). The channel consists of undoped narrow-band (t_1) region and two wide-band (t_2) regions. Region $t_1 = 4$ nm uses $In_{0.53}Ga_{0.47}As$ region, $t_2 = 1$ nm uses InP. Source/drain region doping is 10^{20} cm^3 with 5 nm length. The gate length $L_g = 18$ nm, oxide thickness $t_{ox} = 1.2$ nm and body thickness $t_{Si} = 6$ nm.

Gate underlap used in these devices is revealed to be inevitable in nanoscale MOSFETs to minimize short channel effect, to decrease OFF state current and to minimize gate delay [10]. The gate underlap also helps in reducing the parasitic capacitances significantly, thus resulting in higher speed and lower power dissipation. As the underlap length (L_{un}) is increased, coupling between source and drain is reduced considerably, particularly for a shorter channel length, which, in turn, causes OFF state leakage to reduce. On the other hand, increase in underlap causes increases in the series resistance of the channel, degrading the ON performance [11]. A considerable improvement of ON-OFF ratio with an increase in L_{un}, is a clear indication of improved OFF state control, which is much more prominent for the shorter length devices.

3. Device simulation result

The 2D device simulation is done using Sentaurus TCAD. The density gradient model used in the simulation, solves the quantum potential equations self consistently with the Poisson equation and carrier continuity equations. The quantum potential is introduced to include quantization effects in a classical device simulation. Density gradient transport model is used mainly in simulating nanoscale devices, such as single gate MOSFET's, double gate MOSFET, FinFET and underlap structures. Quantization effects is used to analyze the carrier transport in the interface between the two dissimilar band-gap semiconductor material [12]. Extensive simulation has been done by varying underlap length L_{un} and interface states D_{it} for both devices.

III-V compound semiconductor devices are often benchmarked against the presently prevailing silicon devices for determining performance enhancements. There are four major device metrics to evaluate the emerging devices:

1) intrinsic gate delay versus gate length L_g,

2) energy-delay product versus L_g,

3) subthreshold slope versus L_g,

4) delay versus I_{on}/I_{off} [13].

These four metrics provides the four essential device parameters for logic applications: 1) speed, 2) switching energy, 3) scalability, 4) off state leakage [13].

Fig. 2, show $I_D - V_g$ (drain current versus gate voltage) characteristics, for both devices with constant $L_g = 18$ nm and $L_{un} = 5$ nm. We can find excellent characteristics clearly depicting higher drain level for III-V heterostructure

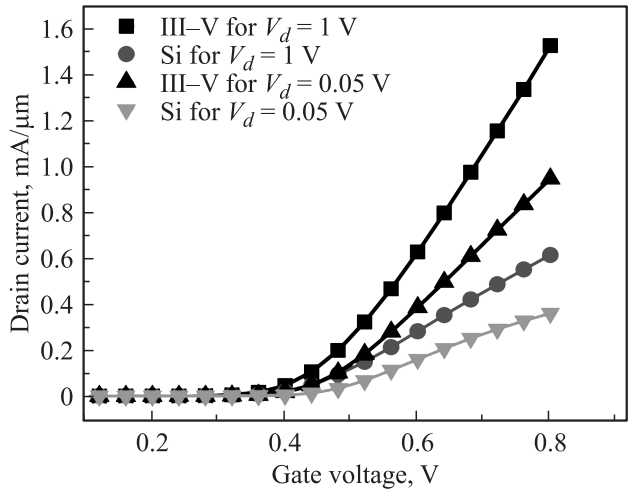

Figure 2. I_D versus V_g characteristics of both devices, with constant gate length $L_g = 18$ nm, body thickness $t_b = 6$ nm and underlap length $L_{un} = 5$ nm. The applied drain voltage is $V_d = 0.05$ V and $V_d = 1$ V for both devices.

device, arising from high mobility and conductivity than silicon. We observe good drain current saturation arising from considerably lower EOT, with double gate providing much better channel control [7]. High electron mobility and conductivity leads to higher drive current at both low drain and high drain bias, which are of great significance for high speed logic applications. The linear drive current (low drain bias) is directly proportional to the conductivity and the saturated drive current (high drain bias) is proportional to the carrier density, as well as the carrier injection velocity. The carrier injection velocity in turn depends on the low-field carrier mobility and effective mass m^* [9].

Important parameter describing electrostatic integrity of MOSFETs is drain induced barrier lowering (DIBL), which is expressed as the shift of threshold voltage due to change in the drain voltage. The DIBL can be calculated as DIBL $= [(V_{th1} - V_{th2})/(V_{ds1} - V_{ds2})]$ where V_{th1} and V_{th2} are threshold voltages extracted at drain bias of $V_{ds1} = 50$ mV and $V_{ds2} = 1.0$ V. DIBL for varying L_{un} and L_g is shown in Fig. 3. DIBL for III-V heterostructure is very impressive as compared to silicon, showing better gate control and improved SCE.

Interface states (D_{it}) arise at the interface of III-V material and dielectric leading to degradation of subthreshold slope and transport properties. Simulation is done using an exponential distribution of D_{it} at the interface with the $D_{it} = 10^{14}\,\mathrm{eV^{-1}cm^{-2}}$ at the band edges and midgap $D_{it} = 10^{14}\,\mathrm{eV^{-1}cm^{-2}}$ [14]. The interface between narrow-band and wide-band III-V materials is assumed to be defect free. Fig. 4 shows subthreshold slope (SS) variation with L_{un} for various values of L_g, for both devices. The subthreshold slope can be evaluated as SS $= \Delta V_g/\Delta(\lg I_D)$. As seen from the results, heterostructure devices have higher subthreshold slope value than the silicon counterpart. The degradation in subthreshold slope value is because of lower electrostatic control as the channel is away from the gate dielectric interface. Also, materials having high mobility and high permittivity in general causes, higher short channel effects [14]. The sensitivity of subthreshold slope decreases for higher underlap lengths.

I_{on}/I_{off} ratio is a commonly evaluated merit for current CMOS technology. This ratio has significant impact on the static power consumption in low standby power applications. Higher value of I_{on}/I_{off} ratio is desirable. Fig. 5 shows I_{on}/I_{off} ratio variation with gate length for both devices. III-V heterostructure has lower value as compared with Si device, due to higher I_{off} value, which is attributed

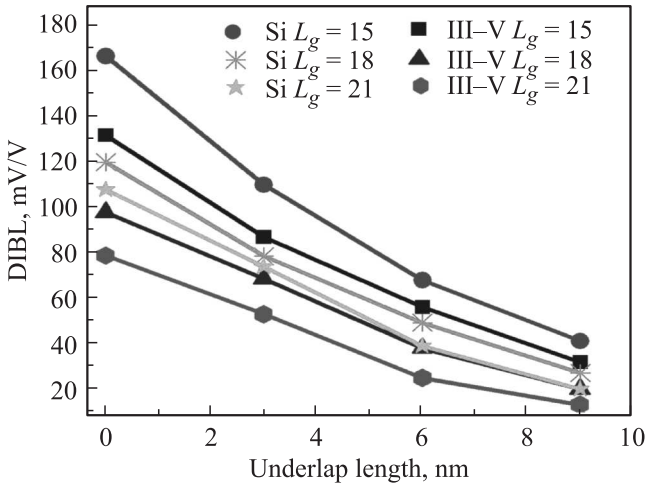

Figure 3. Dependence of DIBL on underlap length L_{un}, for both devices. The gate length L_g is varied from 15 to 21 nm in steps of 3 nm.The underlap length L_{un} is varied from 0 to 9 nm in steps of 3 nm. DIBL $= [(V_{th1} - V_{th2})/(V_{ds1} - V_{ds2})]$ where V_{th1} and V_{th2} are threshold voltages extracted at drain bias of $V_{ds1} = 50$ mV and $V_{ds2} = 1.0$ V.

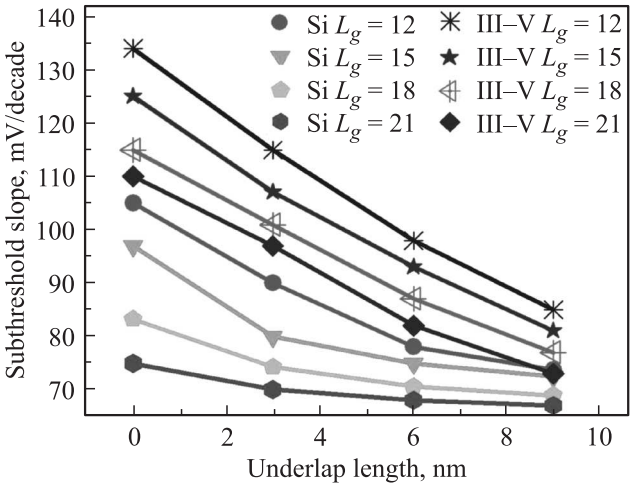

Figure 4. Subthreshold slope versus underlap length L_{un}, for both devices. The gate length $L_g$is varied from 12 to 21 nm in steps of 3 nm. The underlap length L_{un} is varied from 0 to 9 nm in steps of 3 nm. SS $= \Delta V_g/\Delta(\lg I_D)$.

to higher leakage current. Thus optimization of III-V devices for reducing leakage needs to be done.

Intrinsic delay of MOS device is given by $\tau = CV/I$, where C is the total gate capacitance (including parasitic gate overlap and fringing capacitance) per micron transistor width, V is the power supply voltage (V_{dd}), and I is the saturation drive current per micron transistor width ($I_{d\,sat}$); τ is a good metric for device switching speed. Intrinsic delay depends on mobility and carrier injection velocities, which are high in case of III-V materials, thus the intrinsic delay will be less than silicon and these devices will switch much faster than silicon counterpart. Fig. 6 shows delay versus gate length for both devices. III-V heterostructure has lower delay, by virtue of higher mobility.

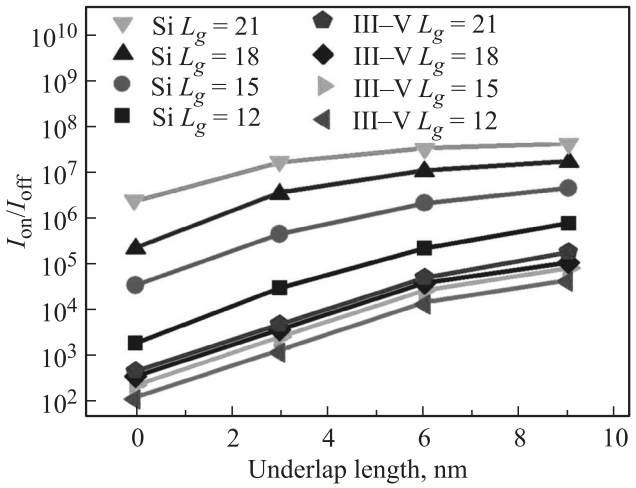

Figure 5. I_{on}/I_{off} ratio variation with underlap length L_{un}, for both devices. The gate length L_g is varied from 12 to 21 nm in steps of 3 nm. The underlap length L_{um} is varied from 0 to 9 nm in steps of 3 nm.

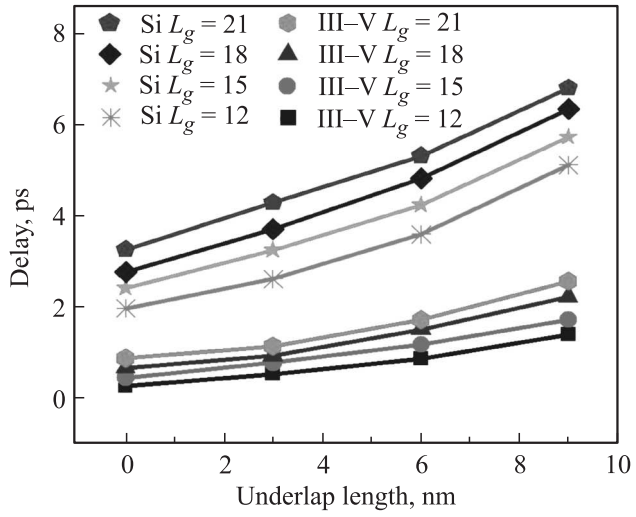

Figure 6. Intrinsic delay variation with underlap length L_{un}, for both devices. The gate length L_g is varied from 12 to 21 nm in steps of 3 nm. The underlap length L_{un} is varied from 0 to 9 nm in steps of 3 nm. Delay $= CV/I$.

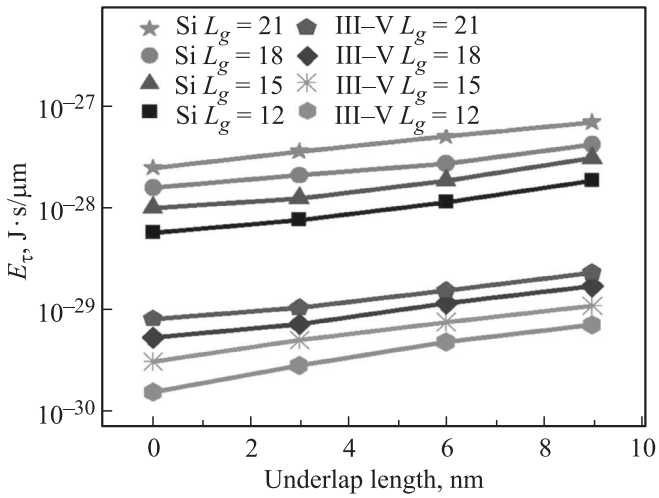

Figure 7. Energy delay product versus underlap length L_{un}, for both devices. The gate length L_g is varied from 12 to 21 nm in steps of 3 nm. The underlap length L_{un} is varied from 0 to 9 nm in steps of 3 nm. Energy delay product $E_\tau = (CV/I) \cdot (CV^2)$.

Fig. 7 shows energy delay product as a function of gate length variation for both devices. III-V heterostructure device shows considerable lower energy delay product value. Lower energy delay product is desirable for low power and high performance logic applications.

4. Conclusions

III-V heterostructure underlap DG MOSFETs using high mobility III-V channel materials can be utilized for sub-20 nm regime. Heterostructure underlap devices using narrowband ternary III-V materials, such as $In_{0.53}Ga_{0.47}As$ and wideband InP, with high-K dielectric provides higher ON current, lesser delay, lower energy-delay product and lower DIBL than the silicon based devices. Results indicate that Heterostructure device has good electrostatic control. However, higher SS and lower I_{on}/I_{off} are some of the concerns which need to be addressed. The SS and delay of the heterostructure device was analysed in presence of interface traps. Thus exploitation of high mobility/small bandgap characteristics can be done using novel device structures, such as III-V heterostructure quantum well devices. The major challenges for integrating III-V material into mainstream, are good surface passivation, low parasitic resistance, low parasitic capacitance and silicon platform incorporation.

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