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Thermal limits for AlGaN/GaN heterojunction transistors on diamond substrates

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An analysis of the influence of buffer layer thickness and composition on the thermal properties of AlGaN/GaN heterojunction transistors on diamond substrates was conducted. It was shown that, despite the significantly higher thermal conductivity of diamond substrates, the need to use thicker buffer layers than on silicon carbide substrates, in particular an AlGaN layer of approximately one micron thickness, can lead to virtually the same active region overheating temperatures while significantly reducing the average transistor temperature.

Keywords: GaN field-effect transistor, channel temperature, diamond substrate.

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A rapid progress has been achieved in recent years in the area of development of field-effect transistors based on gallium nitride heterostructures [1–5]. One of the key advantages of AlGaN/GaN-heterostructure consists in its compatibility with SiC growth substrates, which have a very high thermal conductivity for a semiconductor material (estimated at 350−490 W/(m · K) at a temperature of 300 K depending on SiC polytype). The only physical constraint precluding one from exploiting the full potential of these substrates is the relatively low thermal conductivity of gallium nitride thin layers — around 110−150 W/(m · K) [6,7]. Even though there is data available that confirms it may be much higher: 220−260 W/(m · K) [8,9]. That way even at relatively small thickness of GaN layer equal to 0.5 μm, the maximum temperature in the transistor channel increases noticeably (by 40−50 %) even without transition resistances (Kapitza resistances) at hetero-interfaces or simply sharp boundaries of different materials. Despite perfect thermal conductivity of SiC growth substrates, they are expensive, and their wide practical application is complicated by certain technological difficulties in processing. It is presumed that these problems may be avoided, and heat removal from the transistor active region may be improved significantly by transfer of AlGaN/GaN-heterostructures to growth substrates of diamond [10,11], and this area is being developed actively in recent years, even though no meaningful progress has been achieved in the instrument performance. It is also presumed that initially a heterostructure transferred onto a diamond will be grown on silicon growth substrates and have all specific features of a buffer. In its turn, heterostructures with superb electrophysical characteristics having a thin GaN-buffer may be grown on a SiC growth substrate. Moreover, in paper [12] GaN/AlN-heterostructure was in fact grown with a negligibly small buffer thickness. At the same time, when AlGaN/GaN-heterostructures are grown on silicon growth substrates, the buffer usually has to be made with a thickness of around 2 μm, using at the same time the AlGaN layers with a knowingly lower thermal conductivity [7], even though there is data on using very thin buffer layers as well [13]. The purpose of this paper is to theoretically assess the impact of buffer structural features at thermal properties of AlGaN/GaN-transistors.

The estimates were made for an idealized (without electrodes and grounding holes) planar structure of the transistor, the active region of which contains eight sources of heat and is located away from the side facets of the crystal at 200 μm, which corresponds to the standard topology of a powerful transistor in the centimeter range of wavelengths with eight gates. For convenience of assessments, the temperature at the lower facet of the crystal was set as equal to zero. In this case the temperature produced in the calculations matched the transistor superheating. According to the calculations [14], the main contribution to the heating of both homo- and heterostructure field-effect transistors is made by a narrow region between a gate and a drain of the instrument, where the intensity of heat release exceeds by an order of magnitude the intensity of heat release in other regions of the transistor. For heterostructure AlGaN/GaN-instruments the dimensions of this area of heatrelease are approximately 0.1−0.25 μm.

The size of the region of maximum heat release and its position between the gate and the drain may depend on the mode of instrument operation and features of the transistor structure. Besides, in the area of heatrelease as such the distribution of thermal sources is highly inhomogeneous. At the same time, the neglection of the substantial difference in the dimensions of the maximum heat release region from the source−drain distance may result in minor errors in definition of the critical modes of operation of the instrument (see, for example, [11]). A separate and a very important issue is the impact of transient heat resistances at the thermal properties. This issue is discussed in the detailed paper [15], however, its author neglected the accounting for the actual dimensions of the heat release region.

In thus paper solving the stationary equation of thermal conductivity led to the following values of the heat release region (heat source) in 3D calculations: height $h = 0.05\,\mu$m, length $l = 0.20\,\mu$m, and width W corresponded to the width of the single gate of the transistor. Besides, the heat sources were located directly above the crystal surface at the distance corresponding to the distance between the single gates in the transistor (structure period). The dependence of the thermal conductivity coefficient on temperature was not taken into account.

The specific capacity of the heat sources in the calculations was specified as equal to $Q_0 = 5$ W/mm, which in case of a GaN-instrument operating with the efficiency of $\eta = 50\,\%$, corresponds to its output microwave capacity of $P_{out} = 5$ W/mm.

Temperatures corresponding to other modes of operation of the transistor (η, P_{out}), in virtue of the linearity of the thermal conductivity equation and with account of the adopted approximations may be produced from the values T given in this paper using expression $T_\eta = TP_{out}(100\,\% - \eta)/(\eta Q_0)$.

Thus, for example, for a transistor operating with efficiency of 33 %, at the output capacity of $P_{out} = 5$ W/mm the superheating temperature will double.

Fig. 1 shows the dependences of the maximum temperature in the active region (channel) of the studied transistor with the standard width of a single gate $W = 150\,\mu$m for a powerful instrument of centimeter wavelength range for an AlGaN/GaN-heterostructure on different growth substrates depending on the thickness of the ideal GaN-buffer with thermal conductivity of $\lambda_{\text{GaN}} = 140\,\text{W}/(\text{m}\cdot\text{K})$. The cases with different values of the transient heat resistance between the buffer and the growth substrate have also been considered.

It should be noted that areas of curves with sharp changes of the superheating temperature correspond to small (less than $0.5\,\mu$m) buffer thicknesses.

Let us analyze the produced dependences for the case of absence of the transient heat resistance between the buffer and the growth substrate. As it should have been expected, maximum superheating of the instrument on the silicon growth substrate $\left(\lambda_{\text{Si}} = 150\,\text{W}/(\text{m}\cdot\text{K})\right)$ did not depend on the buffer thickness. For the instrument on the SiC-growth substrate $\left(\lambda_{\text{SiC}} = 490\,\text{W}/(\text{m}\cdot\text{K})\right)$ as the thickness of the buffer increases from 0.1 to $3\,\mu$m, superheating temperature increases by 60 %. For a transistor on a diamond growth substrate with the maximum possible, and rather overstated thermalconductivity for a polydiamond $\lambda_{\text{C}} = 2000\,\text{W}/(\text{m}\cdot\text{K})$ the superheating temperature with the increase in the thickness of a GaN-buffer from 0.1 to $3\,\mu$m rises by more than 2.5 times.

The picture changes noticeably, when a transient heat resistance appears beyween the growth substrate and the buffer. Even at the values of $R_t = 2\cdot 10^{-9}$ K/W, which corresponds to the transient layer at the buffer–substrate interface with thickness of 2 nm and thermal conductivity of $\lambda = 1\,\text{W}/(\text{m}\cdot\text{K})$, from Fig. 1 you can see how the superheating temperature increases significantly at small thicknesses of the GaN-buffer. If in case of thin buffer layers in the calculations not accounting for the transient resistance the advantage of the instrument on the diamond growth substrate in the superheating was more than 100 %, then at even low heat resistance at the buffer–growth substrate interface it makes less than 70 %, and the increase of the transient heat resistance to the value of $R_t = 10^{-8}$ K/W results in the fact that the maximum superheating temperature increases by less than 40 % when changing from the diamond growth substrate to the carbide-silicon one. Effectively, this simplest calculation already poses a question on the prospects of the papers on transfer of nitride-gallium heterostructures onto diamond growth substrates.

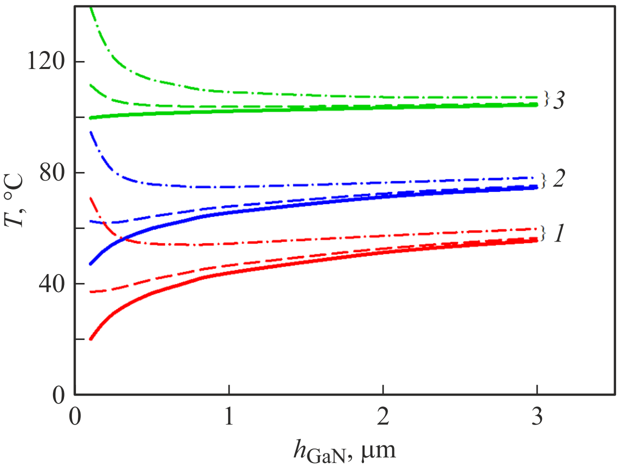

Figure 1. Dependence of maximum superheating temperature in the channel (channel superheating) on thickness of GaN-buffer in transistors on different growth substrates. *1* — diamond, thermalconductivity $\lambda_{\text{C}} = 2000\,\text{W}/(\text{m}\cdot\text{K})$, *2* — silicon carbide, thermal conductivity $\lambda_{\text{SiC}} = 490\,\text{W}/(\text{m}\cdot\text{K})$, *3* — silicon, thermal conductivity $\lambda_{\text{Si}} = 150\,\text{W}/(\text{m}\cdot\text{K})$. Solid lines — transient heat resistance between the buffer and the growth substrate is unavailable ($R_t = 0$), dashed lines — $R_t = 2\cdot 10^{-9}$ K/W, dashed-dotted lines — $R_t = 10^{-8}$ K/W. Thickness of the diamond and carbide-silicon growth substrates is $100\,\mu$m, of silicon one — $50\,\mu$m. The width of the transistor gate is $150\,\mu$m, the distance between the gates is $30\,\mu$m.

Transistors on silicon growth substrates are often made on structures with a thick complex buffer containing AlGaN layers with low thermal conductivity [16]. In virtue of the absence of precise data, let as adopt thermal conductivity of AlGaN layer to be equal to $14\,\text{W}/(\text{m}\cdot\text{K})$ for further calculations, which is exactly 10 times lower than in GaN. In this case, even if the reflection of phonons from sharp interfaces is not taken into account, assuming the layers as such are ideal, the maximum temperature in the channel of the transistor on the diamond growth substrate, the composite buffer of which contains GaN and AlGaN layers with thicknesses of 1.5 and 0.5 μm accordingly, becomes practically the same as the temperature in the channel of the instrument on the carbide-silicon growth substrate with a homogeneous GaN-buffer, and if there are interface heat resistances, even slightly higher (Fig. 2). Besides, the average temperature of such transistor on the diamond growth substrate will be noticeably lower than the average temperature of the instrument on the SiC growth substrate (Fig. 2).

From Fig. 2 it follows that the transistor on the diamond growth substrate has one undeniable real advantage vs. the instrument on the carbide-silicon growth substrate: when the distance decreases between the gate pins, the maximum temperature therein hardly varies (the effect of distributions in Fig. 2), which, possibly, will make it possible to create more compact high-frequency powerful instruments.

Periodically, especially for demonstration of heat removal efficiency, a thermal imager is used in transistors on diamond growth substrates [11,16]. However, the region analyzed by the thermal imager has the size of several micrometers [11], which, generally speaking, is more than not only the specific dimensions of the heat release region, but often than the transistor source–drain distance. This may result in the fact that (especially if you take into account the fact that the metal pins get into the area of the thermal imager spot) when the thermal imager analysis is applied, the maximum temperature in the transistor on the diamond growth substrate (and in fact the temperature averaged by the analysis region size) will be noticeably lower than in the instrument on SiC-growthsubstrate. In fact in the area with the dimensions of the order of micrometer fractions, the maximum temperature that defines degradation in the transistor on the diamond growth substrate may be higher than in the instrument on SiC-substrate, or practically the same. It should also be taken into account that in any analysis of the channel temperature using measurements on the transistor surface, the results will be distorted by the protective coatings on the surface of the instrument.

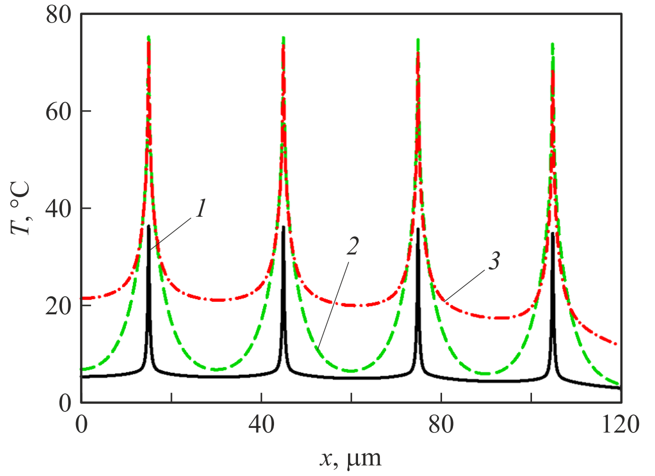

Figure 2. Distribution of superheating temperature in the transistor channel (near the surface of the heterostructure) in the central cross section. *1* — diamond growth substrate and GaN-buffer with thickness of 0.5 μm, transient heat resistance is unavailable, *2* — diamond growth substrate, GaN-buffer with thickness of 1.5 μm and AlGaN layer with thickness of 0.5 μm framed by two layers with thickness of 0.01 μm each with heat resistance of $R_t = 10^{-8}$ K/W each, *3* — carbide-silicon growth substrate, GaN-buffer with the thickness of 1.0 μm and a layer with heat resistance of $R_t = 10^{-8}$ K/W. The width of the transistor gate is 150 μm, the distance between the gates is 30 μm.

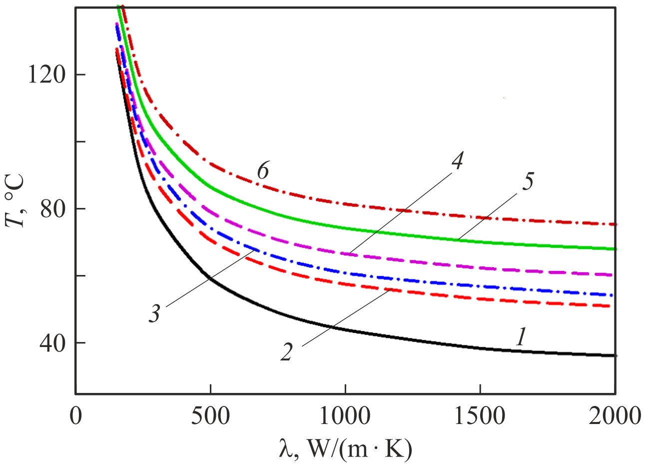

Figure 3. Dependence of maximum superheating temperature in the channel (channel superheating temperature) on thermal conductivity of growth substrate with thickness of 100 μm. Curves *1–6* are explained in the table.

The above assessments were made for an idealized polydiamond with somewhat overstated thermal conductivity compared to the real one, however, it hardly impacts the results, since both for the thick composite buffer and for the thin GaN-buffer the growth of the thermal conductivity of the growth substrate starting from certain values (approximatly 750–1000 W/(m · K)) hardly impacts the instrument overheating (see Fig. 3 and the table).

The obtained results make it possible to conclude that when AlGaN/GaN heterostructure field-effect transistors on diamond growth substrates are made or transferred to such growth substrates, it is necessary to create buffer GaN-layers with thickness of not more than 0.5–1 μm with low (below $2 \cdot 10^{-9}$ K/W) transient buffer–growth substrate resistance. Otherwise, these transistors will not have substantial advantages in thermal characteristics compared to the instruments on the silicon carbide growth substrates. It should be noted that if such breakthrough technology is developed, it should be for certain reasons inapplicable to the instruments on carbide-silicon growth substrates, or the issue of feasibility of transferring to the diamond growth substrates remains open.

Explanation to the curves shown in Fig. 3 (width of the transistor gate 150 μm, distance between gates 30 μm)

Number of curve	Thickness of GaN layer, μm	Thickness of AlGaN layer, μm	Transient heat resistance, K/W
1	0.5	–	–
2	2.0	–	–
3	1.0	–	10^{-8}
4	1.75	0.25	–
5	1.5	0.5	–
6	1.5	0.5	$2 \cdot 10^{-8}$

Conflict of interest

The authors declare that they have no conflict of interest.

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