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Influence of Buffer Layer Design on the Photoluminescence of InAs Quantum Dots Grown on GaAs/Si(100) Substrates

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The synthesis of GaAs layers on on-axis Si(100) substrates using a Si buffer layer is presented. It is shown that the use of an elastically strained $In_{0.1}Ga_{0.9}As$ layer and $In_{0.15}Ga_{0.85}As$/GaAs superlattices, combined with cyclic thermal annealing, makes it possible to obtain relatively thin templates with smooth surfaces and a surface dislocation density of $\sim 8 \cdot 10^7\,cm^{-2}$. Heterostructures with quantum dots based on such buffer layers exhibit photoluminescence at $\lambda \approx 1250$ nm at 300 K and carrier lifetimes comparable to those of similar structures grown on lattice-matched GaAs substrates. The obtained results demonstrate the feasibility of creating efficient light-emitting quantum dot heterostructures on silicon.

Keywords: Indium gallium arsenide, quantum dots in a quantum well, molecular beam epitaxy, semiconductors, silicon, transmission electron microscopy, photoluminescence.

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The integration of optoelectronic components based on direct band gap III–V materials and a silicon platform is considered a promising solution for creating electrically pumped light sources and photonic integrated circuits based on silicon. The most common approach at present is based on direct bonding of silicon and III–V materials semiconductor wafers [1]. Although the efficiency of the method has been demonstrated repeatedly and commercial devices have already been presented, the process itself remains complex and costly. The above-mentioned problems can be overcome by monolithic integration, i.e. direct growth of III–V heterostructures on silicon substrates. It is known that direct growth of III–V materials on silicon substrates is usually marred with the formation of antiphase domains, threading dislocations, and microcracks due to a large lattice mismatch and differences in thermal expansion coefficients [2]. Improving the crystalline quality of III–V layers grown on silicon is usually achieved by growing thick (on the order of $5-7\,\mu m$) buffer layers with multiple filter layers [3], using misoriented Si substrates [4], selective-area growth or migration-enhanced epitaxy [5,6], and so on. However, despite the progress achieved, high material consumption, long process times, technological complexity, and heterostructure cracking remain the primary challenges of these approaches. In this context, considerable attention has been devoted to exploring ways to reduce the overall buffer layer thickness while preserving relevant structural characteristics, and to employing active regions based on arrays of self-organized quantum dots (QDs), which are less susceptible to the influence of dislocations due to spatial isolation of QDs from each other [7]. The present work is focused on investigating the possibilities of synthesis of relatively thin GaAs templates on on-axis Si(100) substrates for subsequent formation of light-emitting heterostructures with InAs/InGaAs QDs based on them.

Sample growth experiments were carried out on a Riber Compact 21EB200 molecular beam epitaxy (MBE) system using 2-inch Si(100) wafers. The system is equipped with a reflection high-energy electron diffraction (RHEED) apparatus and an infrared pyrometer to monitor the surface state and substrate temperature during the structure growth. Substrates were prepared using a modified Shiraki method [8]. RHEED patterns analysis during in-situ thermal annealing of the wafers revealed the formation of a two-domain (2×1) reconstruction at a substrate temperature (T_s) of $T_s = 780\,^\circ C$. In the first growth stage in order to form a smooth surface, a 50 nm silicon buffer layer was grown at $T_s = 600\,^\circ C$ and subsequently annealed at $T_s = 1100\,^\circ C$ to promote step bunching, i.e. the pairing of monatomic steps on the silicon surface [9]. The substrate temperature was then lowered under an arsenic flux to $350\,^\circ C$, and a base GaAs/Si template with a total thickness of 850 nm was grown (Fig. 1); a more detailed description of the growth procedure was presented in Ref. [10].

The morphological properties of the synthesized templates were studied by atomic force microscopy (AFM) using an Ntegra Aura microscope operated in tapping mode with silicon probes (HANC, TipsNano) with a tip

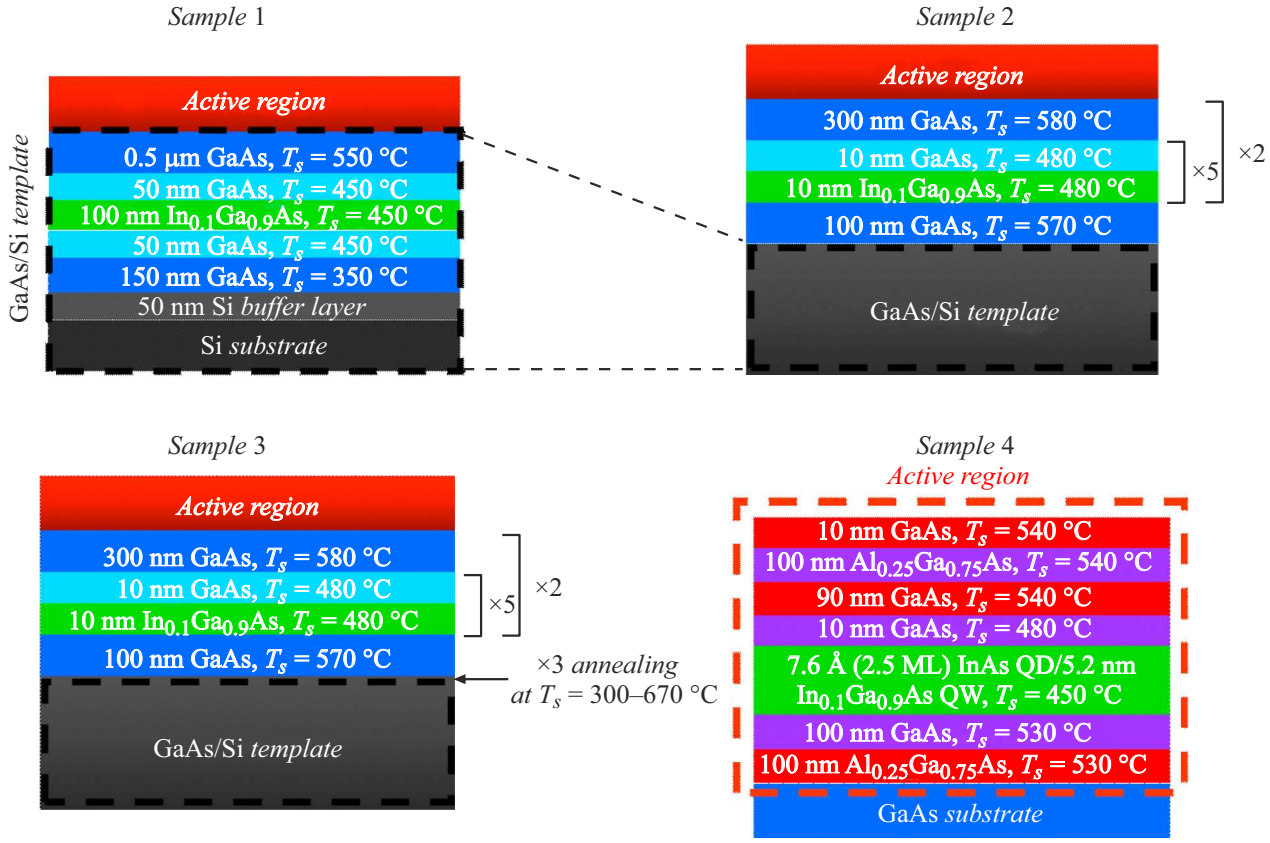

Figure 1. Layer-by-layer structure of samples Nos .1–3 and reference sample No. 4.

curvature radius < 10 nm. The optical properties of the samples were investigated by photoluminescence (PL) and time-resolved photoluminescence (TRPL) at temperatures from 6–293 K. Photoluminescence was excited by a pulsed laser ($\lambda_{ex} = 400$ nm) operating at a frequency of 80 MHz with a pulse duration of 100 fs; the laser spot diameter was 150 μm. Average pump power P_{avg} was varied within the range of 1–100 mW. The structural properties of samples grown on the templates were studied with a JEM2100F (Jeol) transmission electron microscope (TEM) in the (011) transverse cross-sectional geometry at an accelerating voltage of 200 kV. The samples were prepared in accordance with the conventional procedure that includes thinning by precision grinding and sputtering with argon ions to perforation at the final stage.

Following the growth of GaAs/Si(100) templates, cyclic thermal annealing experiments were performed under an arsenic flux ($2 \cdot 10^{-5}$ Torr) [10] at temperatures of 350–700 °C, with the aim of obtaining a smoother GaAs surface and as will be shown below relieving residual strain in the structure. Within one annealing cycle, the substrate temperature was raised to 670–700 °C, held at this level for 5 min, and lowered to 350 °C. The samples subjected to three annealing cycles with a peak temperature of 670 °C exhibited a reduction in root-mean-square (RMS) surface roughness from ~ 2 nm (unannealed) to RMS = 1.4 nm over a 10×10 μm scan area. At the same time, surface degradation due to migration and desorption of Ga atoms from the layer surface was observed at higher annealing temperatures. GaAs/Si templates with a smooth surface were used to grow a series of samples with a single layer of InAs/InGaAs QDs with an emission wavelength around 1.3 μm (Fig. 1). A similar heterostructure with QDs was also grown for comparison on a lattice-matched GaAs(100) substrate.

PL spectra of the synthesized samples are shown in Fig. 2. All of them exhibited room-temperature PL with maxima within the range of 1195–1224 nm, indicating the formation of InAs/InGaAs quantum dots with similar characteristics across all samples. A slight variation of the emission wavelength may be attributed to different degrees of relaxation of the buffer layers and, consequently, different crystal lattice parameters ratios between the matrix and the quantum dots, leading to the formation of QDs of different sizes [11]. Spectral analysis revealed that the lowest emission intensity (approximately 4% of the reference one) corresponded to sample No. 1 grown on a GaAs/Si template with an elastically strained InGaAs filter layer without cyclic annealing. The introduction of two InGaAs/GaAs superlattices (SLs) into the buffer layer led to a significant increase in integrated PL intensity (to 23%). In turn, cyclic annealing of the template prior to SLs formation provided an opportunity to increase the PL intensity of sample No. 3 to 40% of the reference value

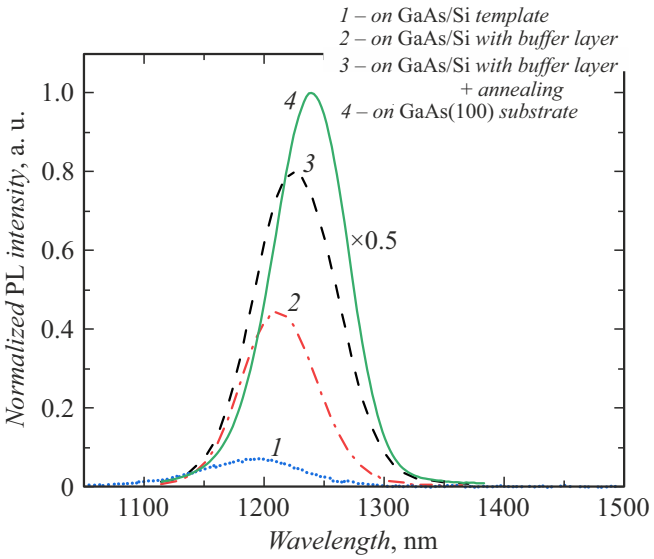

Figure 2. Typical room-temperature photoluminescence spectra of InAs QDs heterostructure grown on various buffer layers: *1* — on a GaAs/Si(100) template with an elastically strained InGaAs layer; *2* — on a buffer layer with 2 InGaAs/GaAs SLs on a GaAs/Si(100) template; *3* — on a buffer layer with 2 InGaAs/GaAs SLs on a GaAs/Si(100) template with cyclic thermal annealing of the template prior to buffer layer growth; *4* — reference sample on a GaAs(100) substrate. The numbers next to curves correspond to the numbers of samples.

without introducing additional dislocation filters. Thus, the progressive increase in integrated PL intensity from 4% to 40% as the strained insertion, superlattices, and cyclic annealing are incorporated into the buffer layer sequentially reflects the contribution of each structural element to the suppression of non-radiative recombination channels.

Time-resolved photoluminescence measurements in order to investigate the optical properties of sample No. 3 in more detail were performed. Figure 3, *a* presents typical decay curves for sample No. 3 corresponding to a monoexponential process for TRPL at 6−77 K. The dependence of the photoluminescence decay time on temperature is shown in Fig. 3, *b*. It can be seen that the decay time at the PL peak wavelength increased from 0.930 ± 0.003 ns at $T = 6$ K to 1.04 ± 0.05 ns at 77 K, which may be associated with a thermally induced redistribution of carriers between quantum dots [12]. It is important to note that such values are typical of decay times observed in QD emission in InGaAs/GaAs systems [13]. The decrease in PL decay time and luminescence intensity at the peak wavelength with increasing temperature up to room one is caused by thermal activation of non-radiative processes at defects located in the vicinity of the QDs.

To study their structural properties, the (110) cross sections of the base template, which included only the InGaAs filter layer and was not subjected to cyclic annealing, and sample No. 3 were examined by TEM. Figures 4, *a*, *b* present the dark-field TEM images of the template and sample No. 3, respectively. The image of the base template (Fig. 4, *a*) reveals the distinct contrast regions that are indicative of the propagation of structural stresses through all the GaAs and $In_{0.1}Ga_{0.9}As$ layers. A redistribution of stresses and their preferential concentration in regions of the elastically strained InGaAs layer and subsequently grown superlattices were observed in the sample subjected to thermal annealing. In addition, one can see the blurring of heteroboundaries of the InGaAs layer after high-temperature annealing, which is caused by the interdiffusion of In and Ga atoms. The density of threading dislocations was determined by counting their number in bright-field TEM images (Fig. 4, *c*). The observed dislocations were predominantly 60-degree ones with Burgers vectors $\mathbf{b} = a/2\,[110]$ (a is the lattice constant); i.e. oriented along directions [110] and $[1\bar{1}0]$. It can be seen that the dislocation density in low-temperature GaAs layers was

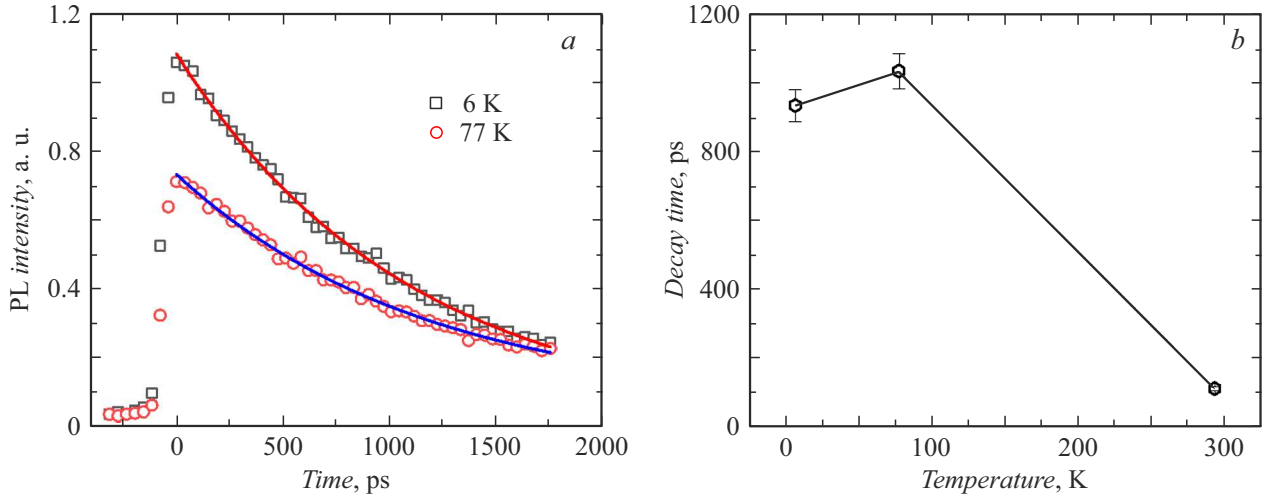

Figure 3. *a* — Experimental PL decay curves at temperatures $T = 6$ K and T = 77 K for sample No. 3 (with approximation) measured at the PL bands maxima. *b* — Dependence of the lifetime on temperature at average pump power $P_{avg} = 100$ mW.

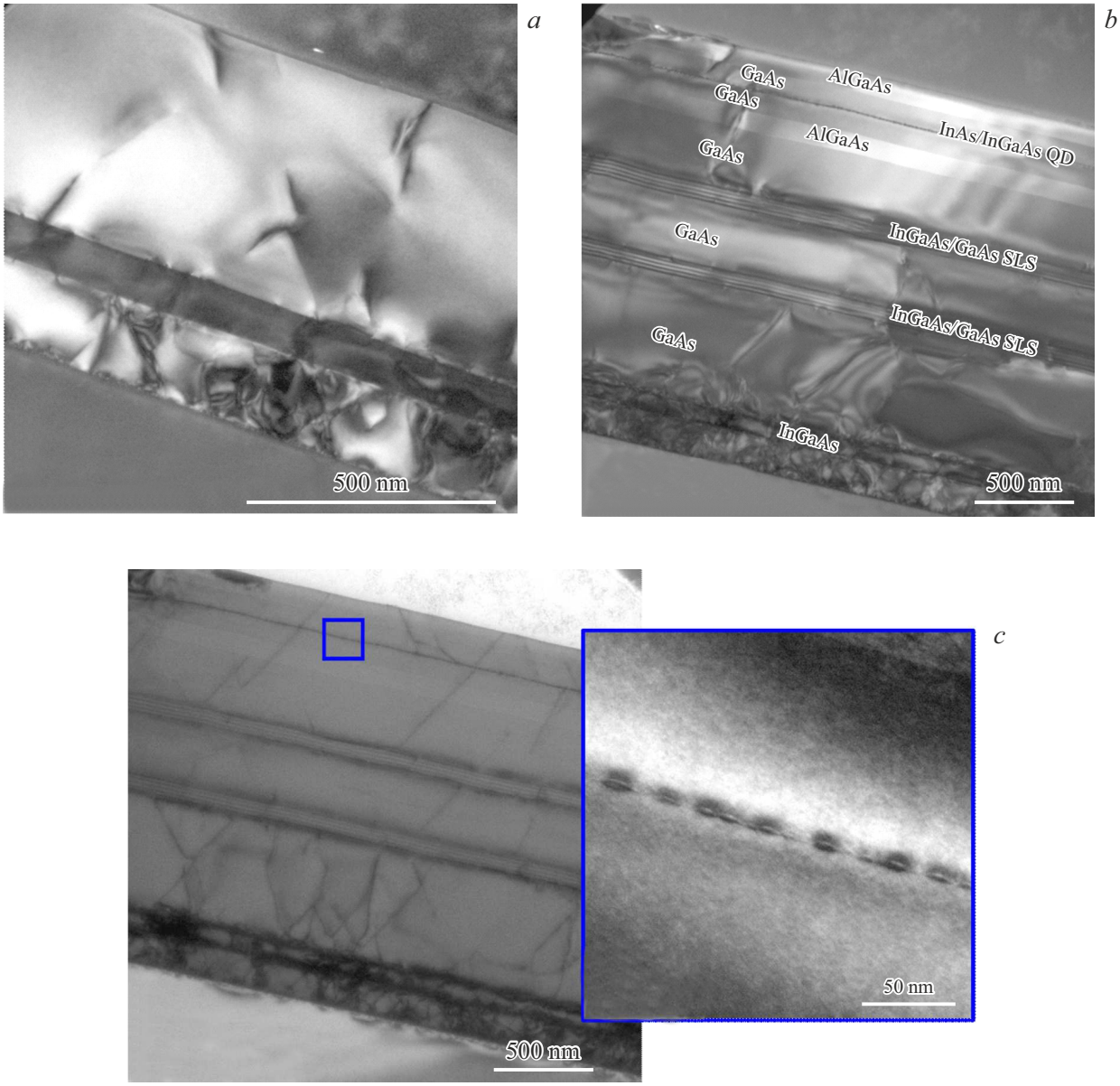

Figure 4. Dark-field TEM images of the (110) cross section obtained using the (002) reflection for the base template with an InGaAs layer without cyclic annealing (*a*) and sample No. 3 (*b*). *c* — Bright-field TEM images of sample No. 3 with an InAs/InGaAs QD-based active region (inset).

$\sim 2.5 \cdot 10^{10}\,\mathrm{cm}^{-2}$ and decreased first to $\sim 8 \cdot 10^{8}\,\mathrm{cm}^{-2}$ after the InGaAs layer within the template. At the same time, combined use of cyclic annealing and two InGaAs/GaAs superlattices in sample No. 3 further reduced the dislocation density after the filter layers to $\sim 8 \cdot 10^{7}\,\mathrm{cm}^{-2}$. Thus, the combination of an elastically strained InGaAs layer and two InGaAs/GaAs superlattices as dislocation filters together with cyclic thermal annealing enables a three-order-of-magnitude reduction in dislocation density within a relatively thin buffer layer. This reduction in threading dislocation density correlates with the increase in PL intensity, which is interrelated with improved crystalline quality of the template. It should be noted that GaAs layers on silicon with a surface dislocation density below $4 \cdot 10^{8}\,\mathrm{cm}^{-2}$ are already suitable for subsequent growth and creating of stripe injection lasers (see recent studies [11,14–16]).

The obtained results verify the possibility of using an elastically strained $In_xGa_{1-x}As$ $(x = 0.1)$ layer and $In_xGa_{1-x}As$ $(x = 0.15)$/GaAs superlattices as dislocation filters in thin GaAs buffer layers on silicon for the growth of light-emitting heterostructures. It was found that the sequential introduction of a strained InGaAs layer, strained InGaAs/GaAs SLs, and cyclic annealing of the structure with a total buffer layer thickness below $2\,\mu$m leads to a step-by-step suppression of dislocation density and a corresponding increase in emission efficiency. It was also

shown that this buffer layer formation method achieves a surface dislocation density of $\sim 8 \cdot 10^7\,\mathrm{cm}^{-2}$ at a smaller overall thickness. Notably, the measured lifetimes of carriers in quantum dots also turned out to be typical for dots in In(Ga)As/GaAs material systems. Thus, GaAs layers obtained by direct growth on on-axis Si(100) substrates may be used for creating light-emitting devices on a silicon platform.

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Conflict of interest

The authors declare that they have no conflict of interest.

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