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Features of measuring the thermal resistance of a microassembly of high-power gallium nitride HEMTs with a silicon MOSFET connected in a cascode circuit

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Received May 07, 2025
Revised May 07, 2025
Accepted October 24, 2025

Thermal electric processes in GaN transistors with a cascode structure consisting of a HEMT and a MOSFET connected in series are investigated. The possibility of determining the HEMT and MOSFET channel resistance based on the results of measuring the current-voltage characteristics of the cascode structure in various switching modes is demonstrated, and estimates of the thermal power dissipated in both crystals are presented. The transistor thermal resistance components were determined using a hardware and software complex implementing a modulation measurement method with heating the object with pulses of a heating current with pulse-width modulation according to the harmonic law. The obtained values of the thermal resistance components are in good agreement with the transistor specifications.

Keywords: gallium nitride transistor, cascode structure, HEMT, MOSFET, thermal resistance, modulation method, thermal radiation.

DOI: 10.61011/EOS.2025.10.62553.8037-25

Gallium nitride (GaN), a widely sought-after material for fabricating high-power and microwave semiconductor devices, exhibits a number of unique properties. High values of electron saturation velocity and electrical breakdown strength have enabled the creation of HEMT transistors (HEMT — high electron mobility transistor) based on this material, operating at frequencies in the tens of gigahertz and delivering output powers in the hundreds of watts [1]. The substantial power dissipated in these transistors necessitates efficient heat removal from the device's active region. A quantitative measure of heat removal efficiency from the active region of semiconductor devices is the thermal resistance „junction−case" R_{Tjc} defined as the ratio of the temperature difference T_j p−n-junction and T_c case of the device to the thermal power dissipated within it [2]:

$$R_{Tjc} = (T_j - T_c)/P,$$

where P — the power dissipated in the device.

The thermal resistance R_{Tjc} determines the maximum allowable dissipated power of the device —- if the power dissipated by the transistor exceeds this limit, thermal breakdown occurs in the transistor structure. Actual values of thermal resistance R_{Tjc} may differ significantly from calculated ones, necessitating precise control of this parameter. Most methods for measuring thermal resistance rely on measuring the transient thermal characteristics (TTC) [3]. During TTC measurement, the transistor is heated by pulses of heating current I_{heat} with durations increasing logarithmically. The junction temperature T_j is measured during pauses between pulses, with a time delay sufficient for the completion of transient electrical processes occurring when switching the transistor from heating mode to temperature measurement mode, via changes in the temperature-sensitive parameter (TSP). For HEMT and MOSFET transistors (metal-oxide-semiconductor field-effect transistor), the on-state channel resistance RDS(on), which varies linearly with temperature, can serve as the TSP [4].

The HEMT structure is continuously refined to improve key electrical, frequency, and energy characteristics. At its initial development stage, HEMTs were normally-on, i.e., the transistor channel was open at gate voltage $U_{GS} = 0$. This posed certain inconveniences for developers of electronic systems using high-power HEMTs. To make them normally-off, an additional $p-n$-junction is formed in the transistor gate circuit [5]. An alternative approach is the cascode structure, in which the HEMT transistor is paired with a low-voltage silicon MOSFET transistor featuring low channel resistance [6]. The HEMT transistor is controlled by the MOSFET gate voltage, while current flows sequentially through the HEMT and MOSFET channels. This complicates the analysis of thermo-electric processes in such a two-chip system, as the on-state resistances $R_{\text{DS(on)}}$ and their temperature coefficients may differ substantially between HEMT and MOSFET.

The subject of investigation was the high-power gallium nitride transistor NTP8G206N manufactured by ON Semiconductor (dissipated power $P_D = 96$ W, drain current $I_{\text{D}} = 17$ A, turn-on delay time $t_{\text{d(on)}} = 6.2$ ns, thermal resis-

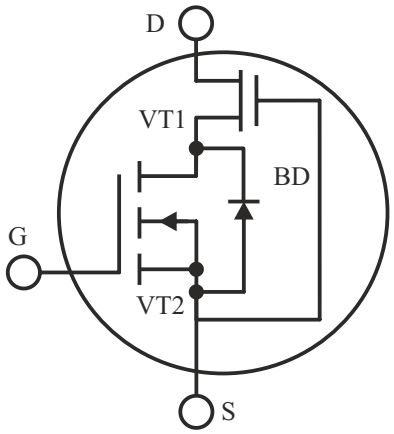

Figure 1. Cascode scheme of a gallium nitride transistor: VT1 — HEMT transistor; VT2 — silicon MOSFET transistor; BD — antiparallel diode.

tance $R_{Tjc} = 1.5\,\text{K/W}$). The transistor features a cascode structure (Fig. 1), comprising the GaN HEMT itself (VT1) and a low-voltage silicon MOSFET (VT2), whose source is connected to the HEMT gate and the latter's source to the MOSFET drain. An antiparallel diode BD (body diode) is included between the MOSFET source and drain; it does not affect normal transistor operation but provides protective functions, e.g., under inductive load.

Transistors with cascode structures typically contain two chips: a GaN chip with HEMT and a silicon chip with MOSFET and antiparallel diode. Occasionally, to enhance transistor performance, an external fast-acting silicon carbide diode is used instead of the antiparallel diode [7]. The chips are mounted in a TO220 plastic package measuring $10 \times 16 \times 4.5\,\text{mm}$. To determine the number and positions of chips in the investigated transistor without package decapsulation, its thermal radiation was measured using the infrared microscope PI 640 (Fig. 2).

The thermogram in Fig. 2, *a* was obtained by passing a current pulse of $I_{\text{heat}} = 5\,\text{A}$ with duration $\tau = 300\,\text{ms}$ from source to drain at gate voltage $U_{\text{GS}} = 0\,\text{V}$, i.e., with the MOSFET channel closed. From the temperature distribution profile shown below the thermogram, it follows that during current pulse flow through the antiparallel diode and HEMT channel, both chips heat up approximately equally, and no third chip with a silicon carbide diode is present in the device.

The thermogram in Fig. 2, *b* was obtained with the MOSFET channel open ($U_{\text{GS}} = 6\,\text{V}$) and a current pulse of $I_{\text{heat}} = 10\,\text{A}$ and $\tau = 100\,\text{ms}$ flowing from drain to source through the series-connected HEMT and MOSFET channels. In this case, one chip heats up noticeably more, due to the difference in HEMT and MOSFET channel resistances. Accurate determination of thermal resistance for both chips requires knowledge of both channel electrical resistances.

The HEMT channel resistance can be determined from analysis of the transistor's current-voltage characteristic (CVC) during current flow from source to drain with the MOSFET channel closed ($U_{\text{GS}} = 0$). In this case, current flows through the antiparallel diode and HEMT channel. The voltage U_{SD} comprises the diode $p-n$-junction voltage, which for silicon diodes ranges from 600 to 800 mV, and the voltage drop across the HEMT channel. The diode CVC is described by the Shockley formula [8]:

$$I = I_{\text{S}}[\exp(qU/mkT) - 1], \tag{1}$$

where I_{S} — saturation current, m — diode $p-n$-junction nonideality factor, k — Boltzmann constant, T — absolute junction temperature.

At $qU/kT > 8$ the unit term in formula (1) can be neglected, and with $m \approx 1$ [8], the diode CVC in semilogarithmic scale is linear:

$$\ln I = lnI_{\text{S}} + qU/kT. \tag{2}$$

According to the datasheet, the NTP8G206N transistor channel resistance is approximately 150 mΩ so at 100 mA current, the voltage drop across the HEMT channel does not exceed 15 mV, much less than across the diode. Therefore, for linear regression (2) calculation (line *1* in Fig. 3), CVC points at $I < 60\,\text{mA}$ were used.

As current increases, the HEMT channel resistance contribution to the transistor CVC grows, requiring replacement of voltage U with $(U - Ir_{CH})$, in formula (1), where r_{CH} — HEMT channel resistance. The measured transistor CVC accounting for HEMT channel resistance drop is shown in Fig. 3 (curve *2*). Comparison of dependencies *1* and *2* yields the HEMT channel resistance. Thus, at $I = 1000\,\text{mA}$ current, the voltage drop difference between diode and transistor is 105 mV (Fig. 3), corresponding to HEMT channel resistance of $r_{\text{CH}} = 105\,\text{m}\Omega$.

From CVC measurement of the investigated transistor with open MOSFET, the total HEMT and MOSFET channel resistance was 132 mΩ implying MOSFET channel resistance r_{CH} of 27 mΩ. Consequently, during thermal resistance measurement, approximately 20% of the heat power generated in the transistor dissipates not in the HEMT but in the MOSFET. This result somewhat differs from [9], where HEMT and MOSFET channel resistances in cascode structures differ by an order of magnitude.

Thermal resistance measurement was performed using the modulation method with object heating by PWM (pulse-width modulation) current pulses varying harmonically [10]. PWM current pulses through the object dissipate variable thermal power $P(t)$ with first harmonic amplitude P_1 causing junction temperature $T_j(t)$ oscillations with first harmonic amplitude T_{j1} phase-shifted by angle φ relative to the power harmonic. The ratio of amplitudes T_{j1} to P_1 gives the thermal impedance modulus Z_{T}, while the ratio of imaginary $\text{Im}T_j$ to real $\text{Re}T_j$ Fourier components of junction temperature at modulation frequency yields the

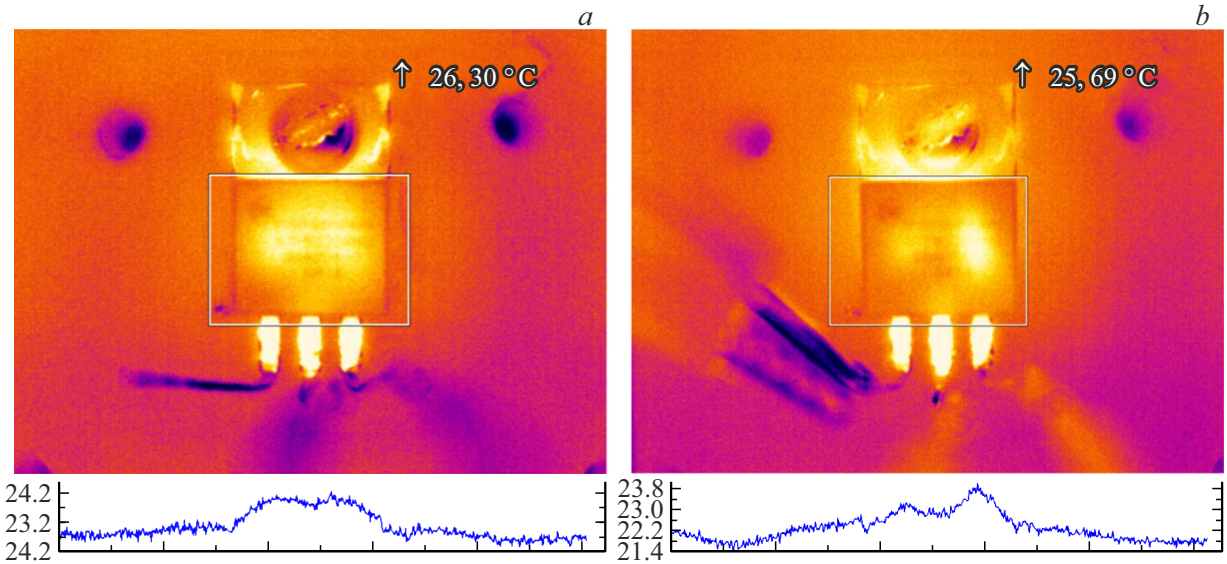

Figure 2. Thermograms of the heated transistor NTP8G206N chips (below are temperature distribution profiles along the axis passing through the chip centers). The maximum temperatures in the field of view are given in the upper right corner of the thermograms. Explanations are given in the text.

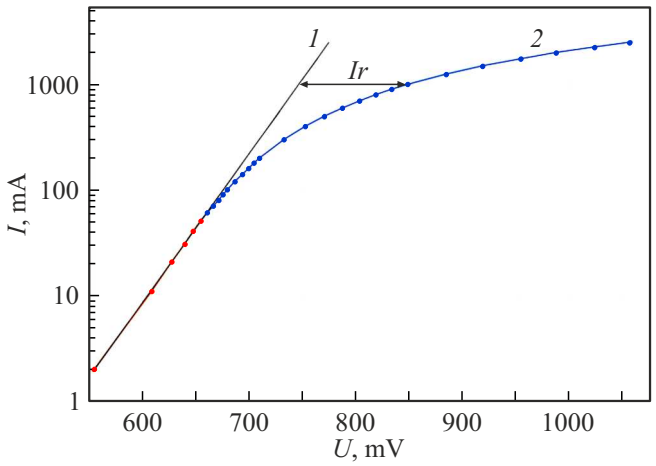

Figure 3. Transistor CVC in semi-logarithmic scale: *1* — diode CVC, *2* — CVC accounting for HEMT channel resistance voltage drop. Explanations are given in the text.

phase tangent φ of thermal impedance:

$$Z_{\mathrm{T}} = T_{j1}/P_1; \qquad \mathrm{tg}\,\varphi = \mathrm{Im}T_j/\mathrm{Re}T_j.$$

By analyzing the dependence of the real part of the thermal impedance $\mathrm{Re}\ Z_{\mathrm{T}}(\nu)$ on the modulation frequency of the heating power, the components of the thermal resistance along the entire path through which the heat flux propagates from the heated channel to the case and further to the heatsink can be determined. The presence of thermal resistance components in the $\mathrm{Re}Z_{\mathrm{T}}(\nu)$ dependence manifests as gentle segments and inflection points, which can be identified through differentiation of $\mathrm{Re}\,Z_{\mathrm{T}}(\nu)$ with respect to the modulation frequency.

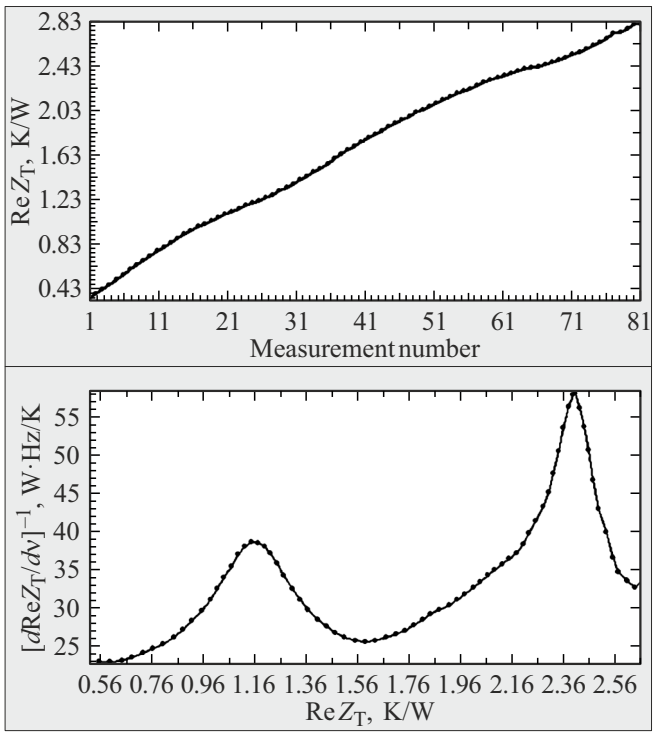

Figure 4. Frequency dependence of the real part of thermal impedance (top) and its processing result (bottom). Explanations are given in the text.

The thermal resistance R_{Tjc} was measured using a hardware-software complex [11] that implements the modulation method. The transistor was heated by PWM current pulses flowing from drain to source through the channels of both the HEMT and MOSFET transistors. The pulse

repetition period was 500 μs. The pulse duration was modulated in the range from 250 to 750 μs. During pauses between heating pulses, with a time delay of 80 μs the temperature T_j was measured via changes in the TSP, whose temperature coefficient is 0.1 mV/K. Measurements were conducted at a heating current of 16,A. The frequency dependence of the thermal impedance was measured in the range from 40 to 0.025 Hz with uniform logarithmic frequency steps (20 points per decade). In calculating the HEMT chip thermal resistance, only the thermal power dissipated in that chip was considered. The results of measuring the dependence of the real part of the thermal impedance $\mathrm{Re}\,Z_\mathrm{T}(\nu)$ on the heating power modulation frequency are shown in the upper panel of Fig. 4. The lower panel shows the dependence $[d\mathrm{Re}Z_\mathrm{T}/d\nu]^{-1}$ on $\mathrm{Re}\,Z_T$. The positions of the maxima relative to the abscissa axis determine the thermal resistance component values. The first component $R_{\mathrm{T1}} = 1.16$ K/W corresponds to the „junction−case„ thermal resistance of the HEMT transistor, which agrees well with datasheet values; the second component $R_{\mathrm{T2}} = 2.40$ K/W — corresponds to the „junction-heatsink“ thermal resistance.

The results presented in this work demonstrate the feasibility of estimating the power dissipated by each chip in the cascode structure, as well as the applicability of the modulation method for measuring thermal resistance components in such transistors.

Funding

This work was supported by the Ministry of Science and Higher Education of the Russian Federation under the state assignment of the V.A. Kotelnikov Institute of Radio Engineering and Electronics of the Russian Academy of Sciences (FFWZ-2025-0001).

Conflict of interest

The authors declare that they have no conflict of interest.

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Translated by J.Savelyeva