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Charge accumulation and relaxation in active mode of $Al/Si_3N_4/SiO_2/n$-Si device structures

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Two MIS structures ($Al/Si_3N_4/n$-Si and $Al/Si_3N_4/SiO_2/n$-Si) formed on n-type crystalline silicon substrates grown by the Czochralski method are studied. The substrate has crystallographic orientation (100) with a resistivity of $4.5\,\Omega \cdot$ cm. The layer of silicon nitride (Si_3N_4) is formed by low-pressure chemical vapor deposition (LPCVD) using a gas mixture of ammonia and monosilane. The layer of silicon dioxide (SiO_2) is formed by thermal oxidation of silicon in dry oxygen. The thickness of Si_3N_4 is 70 nm and the thickness of SiO_2 is 5 nm. The current-voltage (I-V) and capacitance-voltage (C-V) characteristics are measured, and the thermally stimulated relaxation of the charge accumulated in Si_3N_4 is studied. It is established that $Al/Si_3N_4/n$-Si structures under applied DC voltage can accumulate both positive and negative charges, while $Al/Si_3N_4/SiO_2/n$-Si structures can accumulate only negative charges. The accumulation of specific charge types corresponds to the dominance of monopolar injection during charge transfer in the structures. The capture of charge carriers (both electrons and holes) in traps within silicon nitride is responsible for switching processes from high electrical conductivity state to low conductivity state. During positive charge relaxation in $Al/Si_3N_4/n$-Si structures, two kinetics are observed, which is associated with the dominance of two types of traps involved in hole capture and charge transfer through the silicon nitride layer. It is shown that the presence of a silicon oxide layer enhances the thermal stability of charge stored in Si_3N_4 by introducing an additional energy barrier for electrons in $Al/Si_3N_4/SiO_2/n$-Si structures. It is established that within the 300–500 K temperature range, the flat-band voltage shift ΔU_{fb} induced by charge relaxation in Si_3N_4 layer does not exceed 20 %. The results of this work can be used in the design of non-volatile memory cells.

Keywords: nonvolatile memory, MIS structures, MNOS structures, electric charge, C-V characteristics.

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Introduction

The main components of non-volatile Electrically Erasable Programmable Read-Only Memory (EEPROM) are MOS (metal/oxide/semiconductor) or MIS (metal/insulator/semiconductor) transistors, in which the process of accumulation of the electric charge [1,2] is realized, for example, MOS structures with a floating gate (made of polysilicon, metal silicides, etc.). Charge carriers accumulate directly in the floating gate in such memory cells. Other types of device structures, whose operation is based on charge accumulation and storage, can be: doped MOS or MIS structures, where charge carriers are trapped on impurity atoms; structures with arrays of quantum dots, in which charge is trapped and retained in the potential wells of the dots; structures with a multilayer insulator, where information is stored by trapping of charge carriers on intrinsic traps in the insulator [1–8].

It should be noted that the most technologically advanced structures of silicon microelectronics for memory cells are structures based on silicon nitride. This is due to the fact that the technological processes of Si_3N_4 formation are well developed. Silicon nitride is used in microelectronics, primarily as a masking coating during technological operations. Memory cells based on Si_3N_4 can be implemented in various configurations: two-layer — metal/silicon nitride/silicon oxide/silicon (MNOS, in the general case metal/insulator/oxide/semiconductor — MIOS) or three-layer — metal/silicon oxide/silicon nitride/silicon oxide/silicon (MONOS). Instead of metal, polysilicon can be used — the so-called SONOS structures, as well as tantalum nitride — TANOS structures [6–10]. Memory cell designs with a greater number of insulator layers have been reported [11].

The advantage of cells containing MONOS-type structures over memory on floating-gate transistors is the lower voltage required for writing a bit of information, less insulator degradation during writing, and greater radiation resistance. Despite a fairly large amount of information [12–14] on the crystal structure and structure of the electronic bands of Si_3N_4, issues related to the mechanisms of charge transfer, its capture and the temperature stability of the accumulated charge continue to be studied.

MIS structures based on Si_3N_4 may be of additional interest for creating memristors [15–19]. In this case, charge transfer occurs from the contact (electrode) to the contact through the insulator layer. The capture of electrons (or holes) on traps in Si_3N_4 can cause the transition of MIS structures from a state with high electrical conductivity to a state with low conductivity. Combining memristor and EEPROM cells opens up additional possibilities for developing memory devices.

The purpose of this work is to investigate the possibility of charge accumulation and its temperature stability in MIS and MIOS structures with silicon nitride to create new semiconductor information storage devices.

1. Experimental procedure

The MIS structures of Al/Si_3N_4/*n*-Si and MIOS structures of Al/Si_3N_4/SiO_2/*n*-Si were studied. The structures were fabricated at JSC „INTEGRAL“ — Holding Management Company „INTEGRAL“ on substrates of monocrystalline silicon grown by the Czochralski method. The substrates are doped with phosphorus, the resistivity is $4.5\,\Omega\cdot$cm. The crystallographic orientation of the wafers is (100). Wafer thickness is $380\,\mu$m. Silicon nitride (Si_3N_4) was obtained by chemical vapor deposition. The gas mixture contained ammonia (NH_3) and monosilane (SiH_4). Deposition was carried out at reduced pressure (LPCVD method). The thickness of the Si_3N_4 layer is 70 nm. Silicon dioxide (SiO_2) was obtained by thermal oxidation in dry oxygen. Process temperature is 800 °C; SiO_2 layer thickness is 5 nm. A schematic representation of the studied Al/Si_3N_4/*n*-Si and Al/Si_3N_4/SiO_2/*n*-Si structures is shown in Fig. 1.

Phosphorus diffusion from the PCl_3 gas phase was carried out in the reverse side of the wafer. Process temperature was 1000 °C, diffusion time was 6 min. The results of the process were monitored by measuring the specific surface resistance, which was $4.55\,\Omega/\square$. Contacts to the back and planar sides of the wafer were obtained by thermal evaporation of aluminum followed by annealing. For contact stabilization and adhesion improvement, additional heat treatment was carried out in a nitrogen atmosphere at a temperature of 400 °C. The thickness of the aluminum layers deposited on the back and planar sides of the wafer is $0.7\,\mu$m. The metallization area on the planar side is $1.85\times1.85\,\text{mm}^2$. After the completion of the technological operations, the wafers were mechanically scribed into chips. Chip area is $2.5\times2.5\,\text{mm}^2$.

Current-voltage (I-V) characteristics were recorded using Keithley 2450 source-measure unit. The measurements were carried out in the voltage source mode in the range from −60 to +60 V. Agilent E4980A (Option 001) and Agilent 4285A LCR meters were used to register the dependences of the real Z' and imaginary Z'' parts of the impedance $Z=Z'+iZ''$ on the alternating current frequency $f=\omega/2\pi$. The measurements were carried out in the frequency range from 20 Hz to 30 MHz at a sinusoidal voltage amplitude of ≤ 40 mV. The impedance measurement error is $\leq 3\,\%$. The capacitance C of the studied objects was calculated according to the methodology described in Ref. [20].

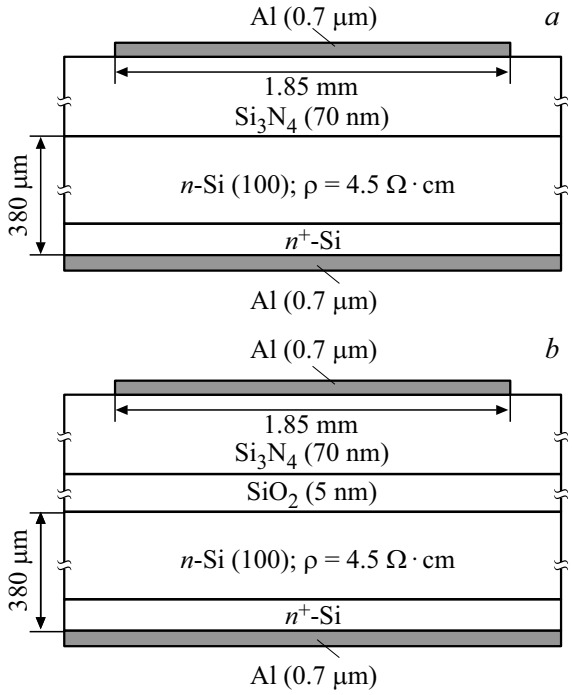

Figure 1. Cross section of the studied Al/Si_3N_4/*n*-Si (*a*) and Al/Si_3N_4/SiO_2/*n*-Si (*b*) structures. The thickness of the layer is indicated in parentheses; (100) is the orientation of the crystallographic plane of *n*-Si substrate. Not to scale.

The capacitance-voltage (C-V) characteristics were recorded at a frequency of $f=1$ MHz. The bias voltage range U used for recording C-V characteristics was from −40 to +40 V, with a bias voltage step of 0.1 V. The positive bias voltage U was considered to be the bias at which a high potential („+“) was applied to the Al electrode from the Si_3N_4 side, and a low potential („−“) was applied to the Al electrode from the *n*-Si side. All measurements were performed under laboratory conditions, in the dark.

A constant bias voltage $U=40$ V ($U=-40$ V) was applied to Al/Si_3N_4/*n*-Si structures for 10 min to study the relaxation of the accumulated charge under isothermal conditions. Next, the structures were maintained for the required time at room temperature in the dark at $U=0$ V. The maximum exposure time is 5800 min (≈ 4 days).

The kinetics of thermally stimulated relaxation of the accumulated charge was studied under isochronous conditions. A constant bias voltage $U=40$ V was applied to Al/Si_3N_4/SiO_2/*n*-Si structures for 10 min. Next, the structures were kept for $\tau=15$ min at a fixed temperature T in the air in a furnace. The temperature T varied in the range of 450−675 K.

Charge relaxation was studied by changing the flat-band voltage, calculated according to the standard method from

C-V characteristics [1,21]. The C-V characteristics were recorded at room temperature in the range of constant bias voltages, which ensures minimal recharging of trap centers in the insulator during the measurement process.

2. Experimental results and discussion

The representation of I-V characteristics in Poole–Frenkel ($\log_{10}(I) - U^{1/2}$) coordinates [1] is used to analyze currents in microelectronic insulator films and, in particular, to determine the conditions for the injection of charge carriers into films. I-V characteristics of Al/Si_3N_4/n-Si and Al/Si_3N_4/SiO_2/n-Si structures in the indicated coordinates are shown in Fig. 2, *a*. It can be seen that, the I-V characteristics of Al/Si_3N_4/n-Si structures sharply increase starting from the voltage of $U_p = 30-35$ V (electric field strength $E_p \approx 5$ MV/cm). The "boundary" voltage is greater for Al/Si_3N_4/SiO_2/n-Si structures, it equals to $\approx 40-45$ V, corresponding to the electric field strength $E_p \approx 6$ MV/cm.

It is known [1] that the type of I-V characteristics of MIS structures depends on the mechanism by which charge carriers overcome the energy barriers existing at the interfaces (injection) and on the mechanisms of charge transfer through the insulator. According to Ref. [1], the main mechanisms determining the passage of charge carriers through the energy barrier at the semiconductor/insulator interfaces are thermal emission and the tunneling effect. Silicon nitride films have a high density of traps in the volume and at the interfaces. Charge transfer through the insulator layer can be described by the Poole–Frenkel model, the multiphonon trap ionization model, etc. [12–14,22]. Hopping conduction via defects in the insulator and resonant tunneling are also possible mechanisms of electron and hole transfer [23–27]. The Poole–Frenkel mechanism is most likely realized in strong electric fields and at low concentrations of traps [1,23–27], in which the main role is played by the reduction of the potential barrier height for carriers trapped at traps (defects that introduce energy levels into the band gap of silicon nitride) under the action of the electric field. As a result, the emission of electrons from the trap levels into the conduction band increases, followed by the realization of the band mechanism of electrical conduction. At high concentrations of defects acting as traps, tunneling between traps becomes possible without emission into the conduction band and subsequent capture [12].

The increase in currents in the initial section ($U < 20$ V) is described by a superlinear dependence. Experimental data can be approximated in the range from 0 to 20 V by a power function $I \propto U^a$ with exponent $a = (1.9 \pm 0.2)$. This is higher than the exponent ($a = 1$), which is characteristic of band conduction due to free equilibrium carriers. The probable reason for this may be the influence of the charge trapped at the traps already at $U < 10$ V. Accordingly, for the studied structures, the change in the type of I-V characteristics is probably attributable to a change in the charge

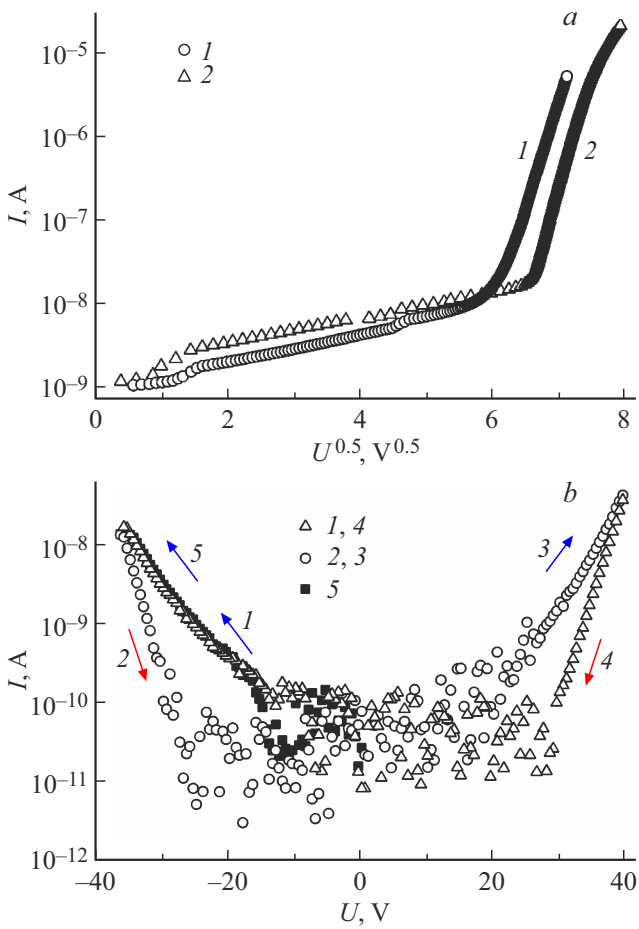

Figure 2. I-V characteristics: *a* — the initial Al/Si_3N_4/n-Si (*1*) and Al/Si_3N_4/SiO_2/n-Si (*2*) structures; *b* — Al/Si_3N_4/n-Si structures during cyclic recording in the range from −40 to +40 V (numbers indicate the sequence of the half-intervals, arrows indicate the directions of U scanning).

transfer mechanism in nitride films: from space-charge-limited currents ($U < U_p$) [1,23–27] to the Poole–Frenkel mechanism at $U > U_p$. The analysis of the I-V characteristics using the Poole–Frenkel mechanism, performed in well-known papers [12–14,23,24], gave contradictory results. At the same time, the authors of Ref. [22] tend to emphasize the significant role of space-charge-limited currents. It should also be noted that to explain the appearance of a state with high electrical conductivity in memristors based on nonstoichiometric silicon nitride, a hypothesis was formulated regarding the formation of „filaments" containing elevated concentrations of silicon and/or metal atoms [25].

The I-V characteristics of Al/Si_3N_4/n-Si structures, cyclically recorded in the range from −40 to +40 V at a temperature of 300 K, are shown in Fig. 2, *b*. It can be seen that structures whose I-V characteristics were recorded during scanning the voltage U from lower (in absolute value) values to higher (dependences *1, 3* and *5*) possess greater electrical conductivity, which can be characterized as a „low resistance state". After changing the direction of U

scanning, the structures have lower electrical conductivity, i.e. they are in a „high-resistance state“. The switching of states observed in cyclically recorded I-V characteristics confirms the influence of charge carriers trapped at traps on the electrical conductivity of the structures. The mechanism of influence is probably identical to the mechanism of space-charge-limited currents. Significant noise in the range from -20 to $+20$ V can be caused by both measurement errors and random recharging of states under conditions of surface potential fluctuations. A significant role of surface potential fluctuations for silicon nitride-based structures was noted in paper [13], and the case of potential inhomogeneity on the surface of a doped semiconductor during the formation of an equilibrium diffusion distribution of electroactive impurity in space charge layers was considered in Ref. [28]. Another reason for the I-V characteristics noise may be the spontaneous (random in time) nature of inversion layer formation.

Since the capture and emission of carriers from traps is a key process in the realization of charge-limited currents, a series of C-V characteristic registrations was conducted to obtain additional information about the carrier localization time at traps. This made it possible to minimize the influence of the external electric field strength on charge transfer. The change in the amount of charge at traps (during its capture and relaxation) is tracked by the change in the flat-band voltage U_{fb}. Externally, the effect manifests itself in a „parallel shift relative to the voltage axis“of the C-V characteristics. Charge relaxation occurs only under the influence of the electric field of the charge itself. The introduction of an additional energy barrier (for example, when comparing Al/Si_3N_4/n-Si and Al/Si_3N_4/SiO_2/n-Si structures) models the reduction of the tunneling probability influence on the charge retention effect.

The flat-band voltage U_{fb} of the initial Al/Si_3N_4/n-Si structures was equal to -2.3 V. The procedures related to measurements during C-V characteristic recording in the ranges from -5 to $+5$ V and from $+5$ to -5 V did not cause flat-band voltage drift. Fig. 3, *a* shows the C-V characteristics of Al/Si_3N_4/n-Si structures, registered in the range of ± 40 V. It follows from the data in Fig. 3, *a* that an increase in the bias voltage to ± 40 V leads to the appearance of a so-called hysteresis. This is manifested in a parallel shift of the C-V characteristics recorded when the scanning direction of the bias voltage is changed from negative values („–“) to positive values („+“) relative to the characteristics recorded when the scanning direction of U is changed from positive values („+“) to negative values („–“). The accumulation of a positive charge can be traced by the displacement of the C-V curve *1* towards negative voltages ($U_{fb} = -9.5\,\text{V} < 0$). The shift of C-V curve *2* towards positive voltages ($U_{fb} = 13.5\,\text{V} > 0$) indicates the accumulation of a negative charge. The plateau on the dependences *1* in Fig. 3 corresponds to the state when an inversion layer is present (formed) in n-Si.

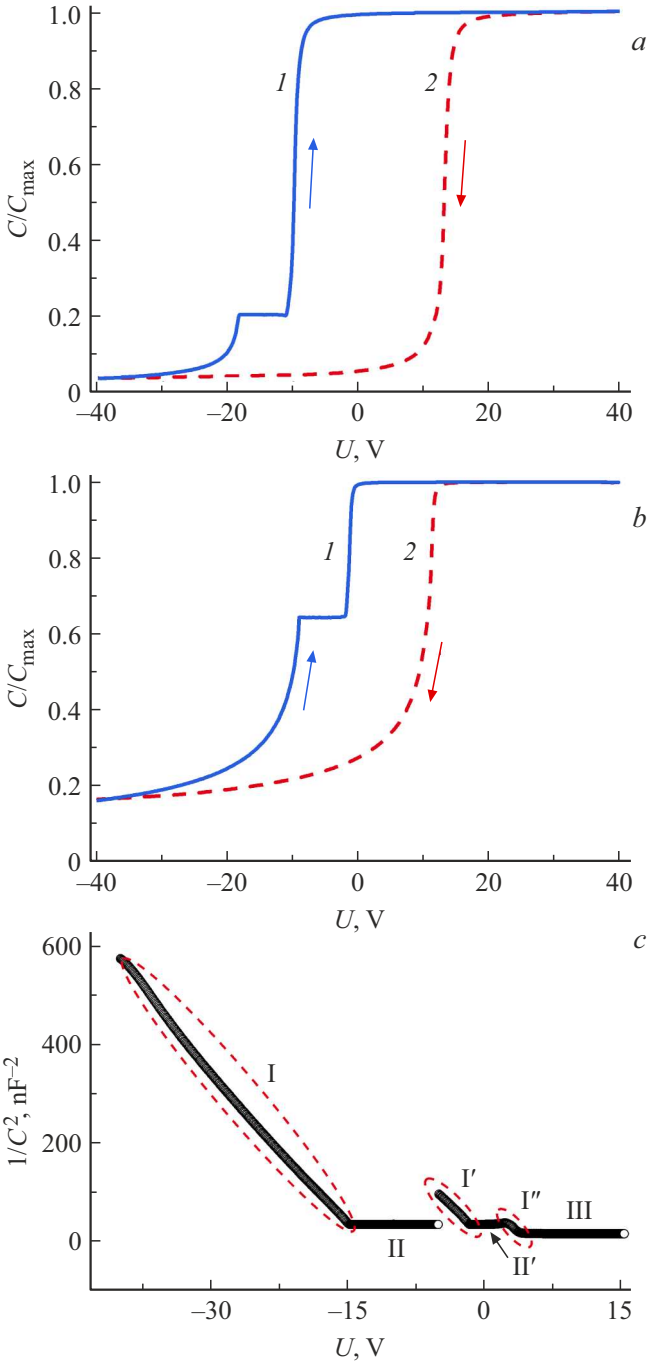

Figure 3. C-V characteristics of Al/Si_3N_4/n-Si (*a*) and Al/Si_3N_4/SiO_2/n-Si (*b*) structures. The dependence *1* was obtained when recording C-V characteristics in the range from -40 to $+40$ V; the dependence *2* was obtained when recording C-V characteristics in the range from $+40$ to -40 V. *c* — C-V characteristics of Al/Si_3N_4/SiO_2/n-Si structures, plotted in $(1/C^2 - U)$ coordinates. For explanations of the characteristic sections, see the text.

It is important that reproducibility of the results is observed with multiple sequential (without time delays) repetitions of registration cycles from „–“ to „+“ and vice versa, i.e. stable reproduction of „hysteresis“ in each measurement cycle. The results of the experiment

with multiple C-V characteristic registration support the hypothesis that Al/Si_3N_4/n-Si structures accumulate both positive and negative charges. The sign of the accumulated charge changes from positive to negative and vice versa cyclically at voltages in the ranges of $(-40)-(-5)$ V and $(+5)-(+40)$ V. The C-V characteristic shift caused by the accumulation of charge corresponds to the dominance of carrier injection of a certain sign: negative — injection of electrons, positive — holes. Thus, when a positive potential is applied to the metal electrode of the Al/Si_3N_4/n-Si structure, electrons are injected into Si_3N_4 from the accumulation layer of n-Si, the injection of holes from the inversion layer is observed in case of application of the negative potential.

The flat-band voltage U_{fb} of the initial Al/Si_3N_4/SiO_2/n-Si structures was -1.1 V. Fig. 3, *b* shows their C-V characteristics. It can be seen that, in contrast to Al/Si_3N_4/n-Si structures, only a negative charge accumulates ($U_{fb} = 12\,\text{V} > 0$). If the bias voltage scanning is limited to intervals from -40 to 0 V (or from 0 to -40 V), no change in the flat-band voltage is observed for Al/Si_3N_4/SiO_2/n-Si samples. The positive charge in the structures does not accumulate, despite the fact that an inversion layer is formed. Another significant difference between the behavior of Al/Si_3N_4/n-Si and Al/Si_3N_4/SiO_2/n-Si structures is that the curve *2* is reproduced with cyclically repeated registrations of C-V characteristics from „$-$“ to „$+$“ and vice versa, i.e. the amount of accumulated charge does not undergo significant changes. The SiO_2 layer serves as an additional barrier and blocks the injection of holes from the inversion layer for Al/Si_3N_4/SiO_2/n-Si structures. A high rate of hole generation „supporting“ the inversion state is required to ensure the injection of holes from the inversion layer. In the absence of illumination, the generation of charge carriers, in addition to deep-level centers, can occur through the participation of surface charge states at the Si_3N_4/n-Si or SiO_2/n-Si interfaces. The density of surface states at the Si_3N_4/n-Si interface is significantly higher compared to the SiO_2/n-Si interface, which likely provides additional conditions for hole injection.

It should be noted, however, that for both types of studied structures, Al/Si_3N_4/n-Si and Al/Si_3N_4/SiO_2/n-Si, during prolonged C-V measurements in the bias voltage U scanning range from -40 to 0 V, spontaneous formation and destruction of the inversion layer was observed. Fig. 3, *c* shows the C-V characteristics of the charged Al/Si_3N_4/SiO_2/n-Si structure, plotted in $(1/C^2 - U)$ coordinates. The charge magnitude was not specifically controlled, the scanning voltage ranged from -40 to $+15$ V. The sections I, I′ correspond to the deep depletion mode, the sections I″ corresponds to the depletion and deep depletion mode (highlighted by dashed ovals). Each of them is approximated by an inclined straight line in $(1/C^2 - U)$ coordinates. Sections II, II′ correspond to the inversion mode, section III′ corresponds to the accumulation mode. In the corresponding voltage ranges, the capacitance remains practically unchanged with changes in the bias voltage. No additional influences were applied to the structure, the measurements were carried out in the dark. In this case, the inversion layer formed and „collapsed“ spontaneously. Thus, the spontaneous formation (and disappearance) of the inversion layer may be the cause of noise in the C-V characteristics shown in Fig. 2. Charge carriers are injected into the insulator from the inversion layer. If the layer has not formed (the structure is in deep depletion mode), injection is unlikely.

The experimental results show that the Al/Si_3N_4/SiO_2/n-Si structures are more preferable from the standpoint of storing the charge accumulated in Si_3N_4 compared to Al/Si_3N_4/n-Si structures. The presence of a SiO_2 layer, which separates Si_3N_4 from n-Si and creates an additional energy barrier, facilitates charge carrier retention at traps.

As a rule, fast and slow processes are conventionally distinguished during the relaxation of the accumulated charge in the MIS structures. Fast relaxation processes are associated with the capture of electrons and/or holes by surface states, while slow relaxation processes are associated with the capture of carriers by traps in the insulator. Fast processes can be studied using relaxation (transient) deep-level spectroscopy (DLTS) [29,30], while slow processes can be studied using C-V characteristic measurement techniques. Preliminary experiments have shown that the sequential registration of C-V characteristics of Al/Si_3N_4/n-Si structures with accumulated charge (regardless of the charge sign) in a narrower voltage range demonstrates a regular shift of the C-V curves and a decrease in the absolute values of flat-band voltage as the time interval t elapsed after charge injection increases. In fact, this means that at room temperature, the Al/Si_3N_4/n-Si structures lose their accumulated charge quite rapidly (within a day). Therefore, a series of C-V characteristic registrations was carried out, which makes it possible to build a time dependence of the flat-band voltage, which illustrates charge relaxation and shows the problematic nature of their use (in the case of the considered design) for memory cells.

Fig. 4 shows two series of C-V characteristics of Al/Si_3N_4/n-Si structures. The first series (Fig. 4, *a*) was obtained for structures with a positive trapped charge, the second series (Fig. 4, *b*) was obtained for structures with a negative trapped charge. As part of the registration of the C-V characteristic series, the structures were kept at room temperature without additional electrical bias ($U = 0$ V). A regular shift caused by the relaxation of the trapped charge is visible for each of the C-V characteristic series. The flat-band voltage shifts from $U_{fb} = -18.2$ V (immediately after injection) to $U_{fb} = -12$ V (after exposure for 22 h) for structures with a positive charge. The flat-band voltage shifts from $U_{fb} = 16.7$ V (immediately after injection) to $U_{fb} = 3.7$ V (after exposure for 4 days) for structures with a negative charge.

The dependence of the flat-band voltage U_{fb} on the time t during the relaxation of the accumulated charge is shown in Fig. 5. It can be seen that, in contrast to the kinetics of relaxation of a positive charge (Fig. 5, *a*), in the kinetics of negative charge relaxation (Fig. 5, *b*) two regions can be

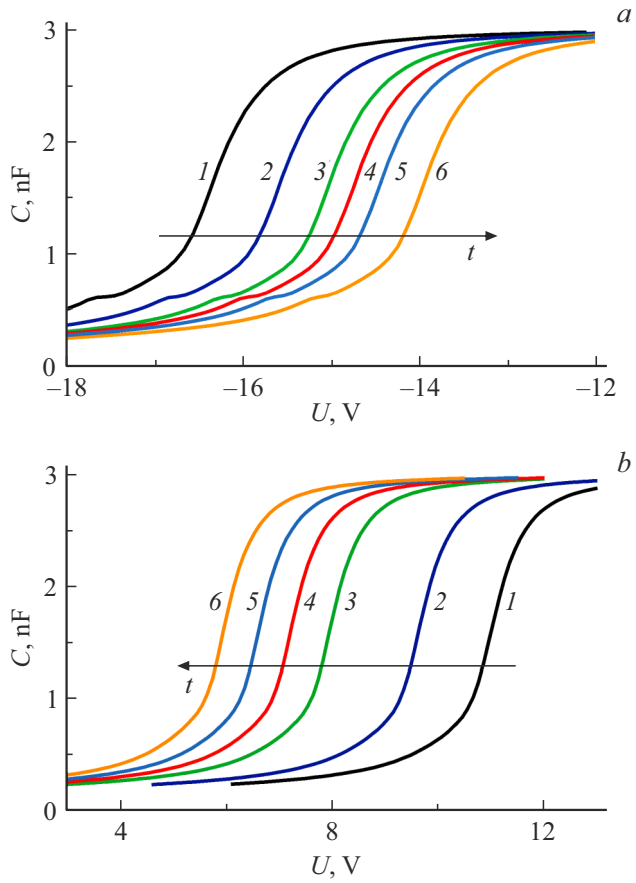

Figure 4. C-V characteristics of Al/Si_3N_4/n-Si structures recorded after injection of positive (*a*) and negative (*b*) charges. The dependences were obtained after exposure at room temperature for $t = 2$ (*1*); 6 (*2*); 13 (*3*); 20 (*4*); 40 (*5*); 60 min (*6*).

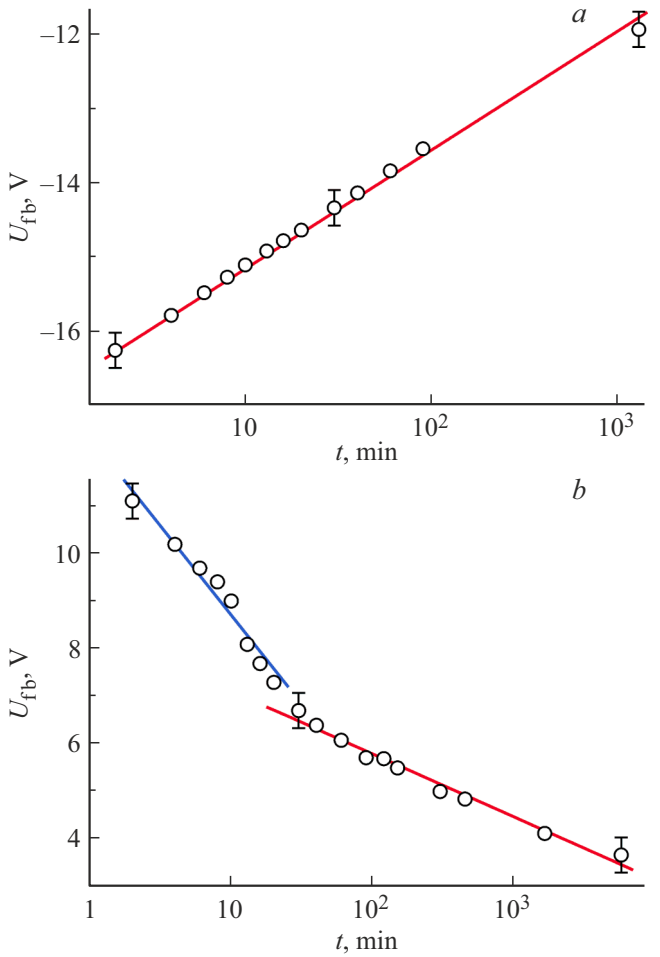

Figure 5. Dependence of the flat-band voltage U_{fb} on the time t elapsed after the injection for Al/Si_3N_4/n-Si structures: *a* — injection voltage $U = -40$ V for 10 min; *b* — injection voltage $U = 40$ V for 10 min.

distinguished, differing in the slope of the $U_{fb} - \log_{10}(t)$ dependence. The structures were maintained without additional electrical bias, so the Al/Si_3N_4/n-Si samples that accumulated a positive charge were in the accumulation mode, while those that accumulated a negative charge were in the inversion mode. Charge relaxation should be associated with the transfer of electrons (holes) through the Si_3N_4 layer. Thus, the presence of two sections in Fig. 5, *b* may either be a consequence of the presence in Si_3N_4 of two types of electronic traps that actively participate in charge capture and differ in the depth of their energy level, or it may indicate the change of the dominant charge transfer mechanism, for example, from the thermal field emission of electrons trapped in the Si_3N_4 layer to the tunneling mechanism [12,13].

It should be noted that the capture and retention of charge in the insulator layer of the Al/Si_3N_4/n-Si structures is one of the causes of the memristor effect. The properties of silicon nitride and memristors based on similar structures have been studied in sufficient detail in Refs. [12–19,22–26] and others. In this context, charge relaxation may hinder the effective implementation of device structures based on Al/Si_3N_4/n-Si. However, if the „read voltage“ does not exceed 1–5 V, as proposed, for example, in Ref. [25], then the Al/Si_3N_4/n-Si structure can retain their state after charge injection for about several hours even without additional technological techniques.

The expected higher charge retention stability was demonstrated by Al/Si_3N_4/SiO_2/n-Si structures. The flat-band voltage of the Al/Si_3N_4/SiO_2/n-Si structures virtually did not change at room temperature for more than a week after they were charged, and the accumulated charge did not change. Conducting an experiment to study charge relaxation over time in Al/Si_3N_4/SiO_2/n-Si structures at standard operating temperatures (up to 75 °C) at this stage of research was considered impractical. Measurements were carried out to determine the range of temperature stability of the charge.

Fig. 6, *a* shows a series of C-V characteristics of Al/Si_3N_4/SiO_2/n-Si structures obtained after isochronous (15 min) exposure at various temperatures. It can be seen that an increase in temperature leads to a shift in the C-V characteristics towards lower U values. A

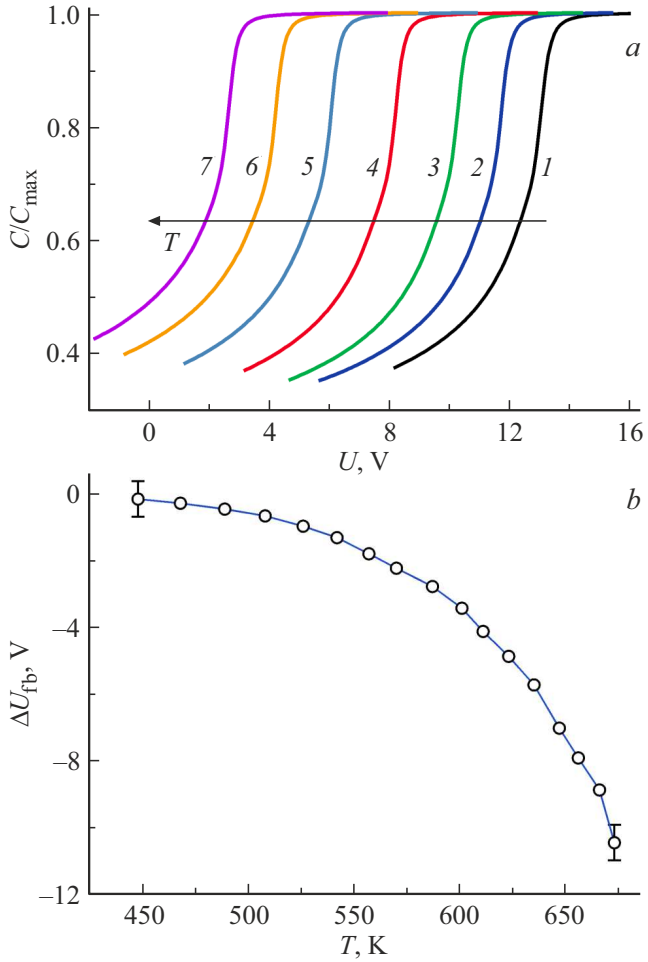

Figure 6. *a* — C-V characteristics of $Al/Si_3N_4/SiO_2/n$-Si structures registered after injection at a temperature of 300 K (*1*) and after exposure at $T = 540$ (*2*); 585 (*3*); 620 (*4*); 645 (*5*); 665 (*6*); 675 (*7*) for 15 min at each temperature; *b* — change in the flat-band voltage ΔU_{fb} due to the temperature of heat treatment T of $Al/Si_3N_4/SiO_2/n$-Si structures.

decrease of the flat-band voltage U_{fb} from $U_{fb} = 13.2$ V (for structures immediately after injection) to $U_{fb} = 2.8$ V (for structures after exposure at $T = 675$ K) is recorded. This indicates relaxation (decrease in absolute value) of the charge accumulated in the insulator. Fig. 6, *b* shows the the flat band voltage values ΔU_{fb} obtained from the C-V characteristics recorded after exposure at various temperatures T. A practically significant (over 20%) decrease of U_{fb} is recorded at temperatures $T > 500$ K. This value approaches the temperatures at which polymer degradation begins. It is higher than the standard operating temperature limit for integrated circuits made on silicon. Thus, the $Al/Si_3N_4/SiO_2/n$-Si structures can serve as the basic structures for the development of non-volatile memory capable of storing information in rather extreme conditions. Structurally, the memory can be made either using EEPROM technology or it can be based on memristors.

Conclusion

It has been found that, $Al/Si_3N_4/SiO_2/n$-Si structures are capable of accumulating only negative charge, unlike the $Al/Si_3N_4/n$-Si structures, which accumulate both a positive and a negative charge when a constant electric voltage in the range from −40 to +40 V is applied to them. Electrons are injected into Si_3N_4 from an accumulation layer of *n*-silicon of $Al/Si_3N_4/n$-Si structures when a positive potential is applied to an aluminum electrode. When a negative potential is applied to Al, holes from the inversion layer are injected into Si_3N_4. The accumulation of charges of a certain type corresponds to the dominance of monopolar injection mechanisms during current excitation in these structures. The capturing of two types of carriers by traps in silicon nitride determines the processes of switching from a state with low electrical conductivity to a state with high electrical conductivity. Upon relaxation of the positive charge, two kinetics are observed in the $Al/Si_3N_4/n$-Si structures, which may be associated with the dominance of two types of traps involved in the capture of carriers of a positive sign and the transfer of this charge through a layer of silicon nitride, and also play a significant role in the formation of space-charge-limited currents. It is shown that the presence of a silicon oxide layer leads to an increase in the temperature stability of the charge accumulated in Si_3N_4 due to an additional energy barrier. It was found that the magnitude of the flat-band voltage shift ΔU_{fb} caused by relaxation of the charge accumulated in silicon nitride does not exceed 20% in the temperature range of 300−500 K.

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Conflict of interest

The authors declare no conflict of interest.

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