Installation for testing avalanche breakdown of field effect transistors operating on an inductive load

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The physical processes in field-effect transistors during avalanche breakdown, including those leading to their destruction, are considered. The dominant is thermal mechanism of destruction which occurs when the temperature of the crystal lattice exceeds the intrinsic temperature of the semiconductor. A method for calculating the peak temperature of the lattice during avalanche breakdown is proposed, which makes it possible to estimate the threshold energy of avalanche breakdown above which the transistor collapses. An installation for testing field-effect transistors at avalanche breakdown energies from 0.5 mJ to 2.5 J has been developed. The installation makes it possible to determine the mechanism of destruction, and the suggested circuit design allows to test both field-effect transistors in a package and chips on uncut semiconductor wafers.

Keywords: Avalanche breakdown, MOSFET and IGBT transistors, thermal destruction of semiconductor devices, testing equipment.

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Power field-effect transistors (FETs) are used widely in various areas of power electronics, which include the design of power supplies and converters, inverters, electronic motor control systems, etc. In most of the listed applications, FETs operate on an inductive load, and when the transistor is turned off, an inductive surge occurs on the drain, which can lead to FET failure.

When the FET switches off, the inductance tends to keep the current in the circuit constant, raising the voltage at the transistor's drain to the avalanche breakdown level $V_{DSS(BR)}$, which is typically 10–30 % higher than the maximum allowed operating drain–source voltage V_{DSS}. Modern field-effect transistors consist of a large number of elementary transistor cells connected in parallel. An „antiparallel" diode (D) and a parasitic bipolar transistor (BJT) are integrated into each cell. Figure 1 shows the cell structure, its equivalent circuit, and the photo of a part of the VDMOS (vertical double-diffused metal-oxide semiconductor) FET structure. The avalanche breakdown (AB) of the reverse-biased diode $p-N$ junction is the factor that limits the voltage spikes at the FET drain. The peak dissipated power may reach tens of kilowatts in this case, and the semiconductor structure undergoes abrupt local heating. It should also be taken into account that with a typical connection of an inductive load between the power supply (V_S) and the FET drain, AB energy E_{BR} may be several times higher than energy E_L stored in the inductive load:

$$E_L = \frac{1}{2} L I_m^2, \tag{1}$$

$$\begin{aligned} E_{BR} &= \int_0^{t_1} V_{DSS(BR)} I(t) dt \\ &= \int_0^{t_1} V_{DSS(BR)} I_m \left(1 - \frac{t}{t_1}\right) dt \\ &= \frac{1}{2} \frac{V_{DSS(BR)}}{V_{DSS(BR)} - V_S} L I_m^2 = \frac{V_{DSS(BR)}}{V_{DSS(BR)} - V_S} E_L, \end{aligned} \tag{2}$$

where V_S is the supply voltage in the FET power circuit and I_m is the current interrupted by the FET that decreases linearly to zero during the time $t_1 = \frac{L I_m}{(V_{DSS(BR)} - V_S)}$. Along with the energy stored in the load inductance, additional energy coming directly from the power supply is dissipated. For example, energy E_{BR} dissipated as a result of AB for an IRF640 transistor with a typical AB voltage $V_{DSS(BR)} \approx 230$ V operating at $V_S = 200$ V is 7.7 times higher than energy E_L stored in the inductive load. Only E_L energy is specified as the maximum AB energy in most FET data sheets, and this fact must be taken into account by circuit designers of FET-based devices with inductive load.

The maximum allowed AB energy is included in the list of basic parameters. Its values for modern power FETs range from several mJ to several J [1–3]. Therefore, testing of FETs for resistance to AB while operating on an inductive load is an essential part of the testing procedure [4–6].

A TM-20/80 setup was designed at the Ioffe Institute in collaboration with Megaimpulse Ltd., for investigating avalanche breakdown processes and testing the resistance of field-effect transistors to avalanche breakdown with the energy stored in an inductive load ranging from 0.5 mJ

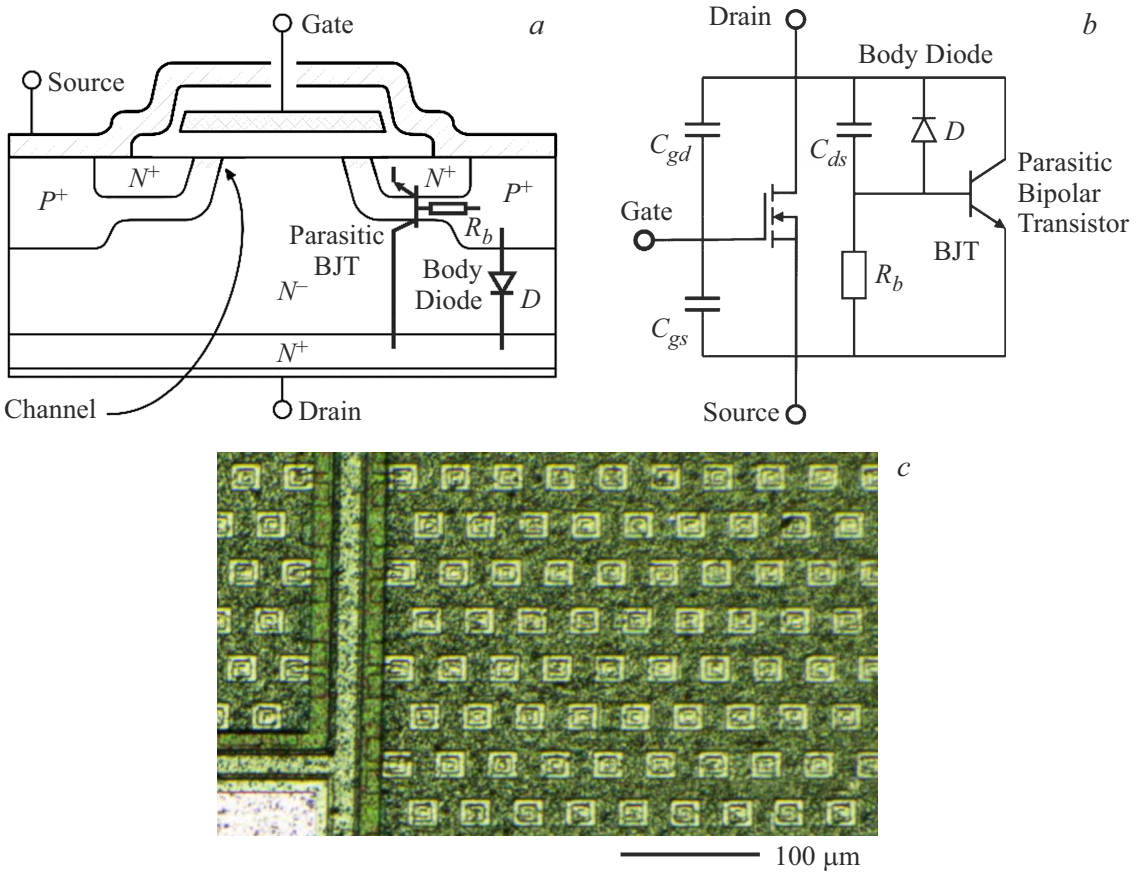

Figure 1. The structure of a field-effect transistor cell (a), its equivalent circuit (b), and photo of the cells in IRF640 field-effect transistor (c). The bus connecting the gates of elementary transistor cells is seen on the left side of the photo.

to 2.5 J (Figure 2, c). These setups were supplied to the production and quality control lines of semiconductor device factory, and they allow testing almost the entire range of N-channel FETs in both manual and automated modes.

Let us examine the process of AB and the mechanism of FET destruction in more detail. Two possible destruction mechanisms are known [7]: spontaneous switching-on and latch-up in the on state of a parasitic bipolar transistor (BJT) (Figures 1, a and b) and thermal destruction of the semiconductor structure. The TM-20/80 setup allows identifying both destruction mechanisms of FETs in avalanche breakdown testing. In addition, the implemented circuit design allows for testing packaged FETs as well as FET chips on uncut semiconductor wafers. For this purpose, a four-wire connection was used to suppress the parasitic inductance of the probes and connecting lines to FET chips.

The simplified block diagram of TM-20/80, which illustrates the principle of its operation, is shown in Figure 2, a. The setup has two power sources: +90 V, which forms a linearly rising current pulse through an inductive load, and an adjustable +24 – +80 V source to check the integrity of drain–source channel of FET under the test (DUT-device under the test). In addition, the setup includes two MOSFET switches $T1$ and $T2$, a DUT driver, a current-measuring shunt $R1$, a relay that disconnects DUT from the setup between test cycles, and a control circuit based on an ATXMEGA64A3-AU microcontroller and an EP3C16E144C programmable logic array. Auxiliary components are not shown in the diagram. The control circuit generates a required sequence of CNT1–CNT4 signals, regulates +24 – +80 V source via DAC, and has DRAIN, GATE, SOURCE+, and SOURCE– inputs for monitoring the DUT drain and gate voltages as well as the current in the power circuit by measuring the voltage drop across $R1$ shunt.

The DUT is connected to the setup by four lines, including two power lines to FET source and drain, a control line to gate, and a gate ground return line connected to source. The DUT driver is galvanically isolated from the power circuit, which helps to eliminate mutual influence between the gate current and the drain–source power current. The relay disconnects all lines to the DUT between tests.

The DUT test cycle includes four stages (Figure 2, b): initial check of gate and drain integrity, controlled current rise in power circuit up to set level, current interruption and AB, final check of DUT gate and drain integrity after AB test. At the first stage, a +10 V pulse is applied to the DUT

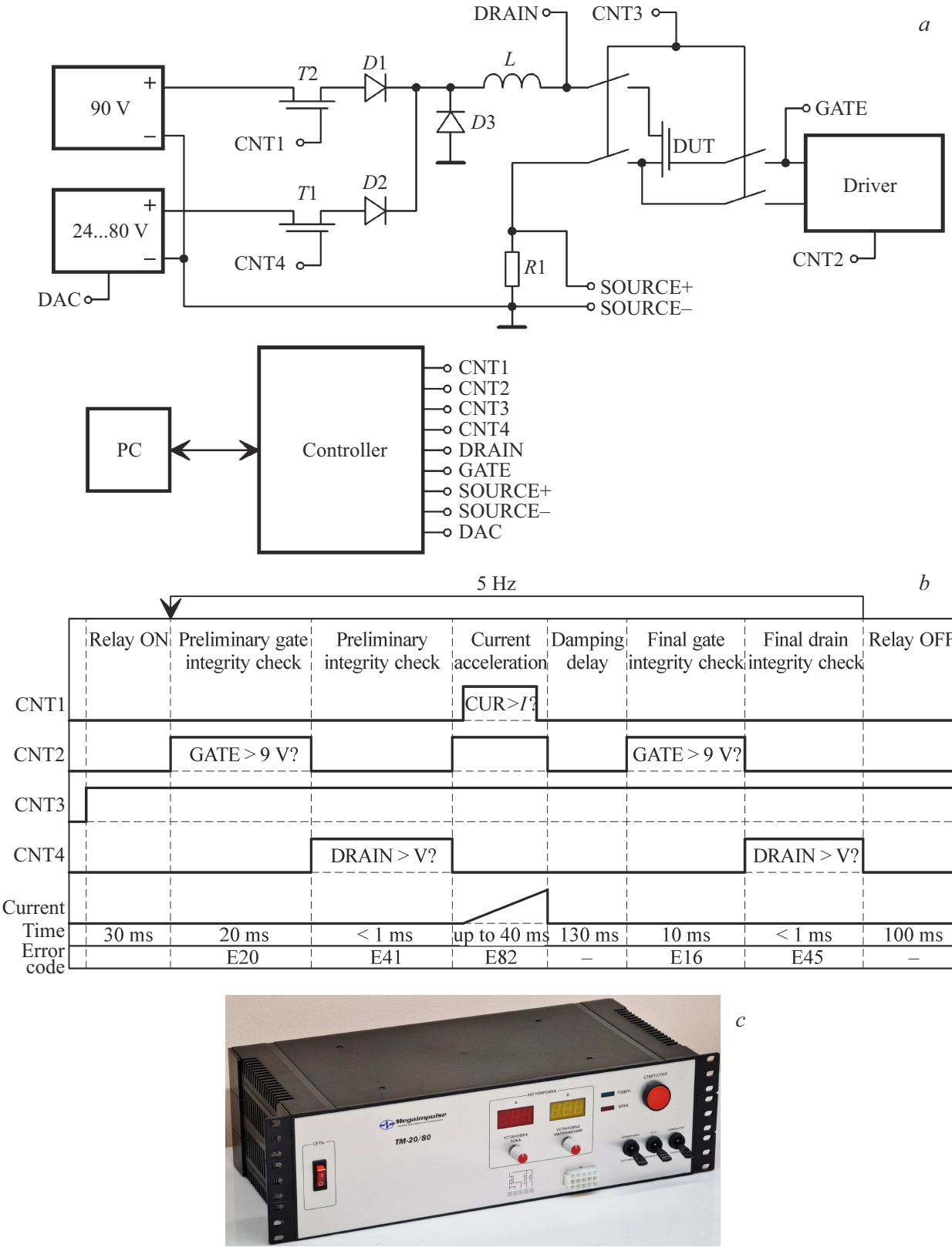

Figure 2. The simplified block diagram (*a*), testing cycle (*b*), and photo (*c*) of the TM-20/80 setup for testing the resistance of field-effect transistors to avalanche breakdown while they are operating on an inductive load.

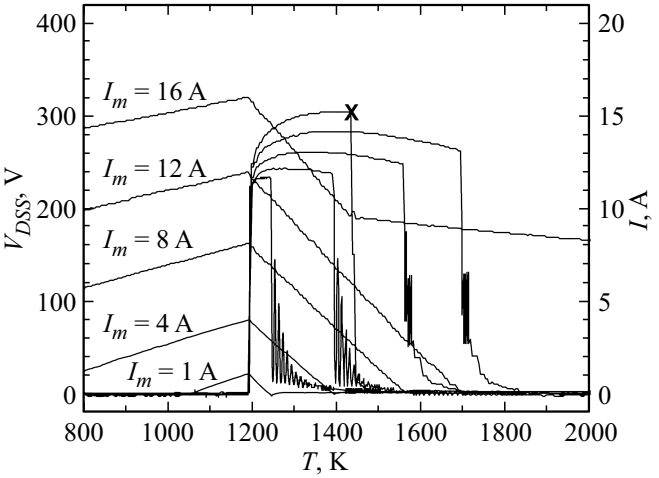

Figure 3. The oscillograms of FET drain voltage and FET current at avalanche breakdown energies from 6.25 mJ ($I_m = 1$ A) to 1.6 J $I_m = 16$ A). The load inductance is 12.5 mH. $V_{DSS(BR),\max}$ increases monotonically with I_m current and avalanche breakdown energy. The cross indicates the moment of thermal destruction of FET. The drain–source voltage drops sharply at this moment, while the current continues to flow through DUT.

gate by CNT2 signal, and then the correct voltage value at the gate is checked after 20 ms. Then, the voltage on the gate is reduced to zero and integrity of the drain–source channel is verified. To do this, the adjustable $+24 - +80$ V source voltage is applied to the DUT drain by CNT4 signal via $T1$ switch, and after the testing of the DUT channel, $T1$ switch is turned off. CNT2 signal turns the DUT on. Then, CNT1 signal turns on $T2$ switch and initiates a controlled current rise through an inductive load, until a current set level is reached. After that, $T2$ switch is turned off, the current through the inductive load is intercepted by $D3$ diode and, after the DUT is turned off, it undergoes AB. At the final stage, the DUT gate and drain integrity are verified again.

The efficiency of the setup operation was tested on IRF640 MOSFETs from International Rectifier. Typical oscillograms of current through DUT and drain–source voltage are shown in Figure 3. The DUT is turned off when the set current is reached, and the drain voltage abruptly increases up to AB level. It can be seen from Figure 3 that DUT passed the AB tests for currents from 1 A to 12 A. However, thermal destruction was observed at a current of 16 A, which resulted in an abrupt reduction of the DUT drain–source voltage, while current continued to flow through it. The TM-20/80 setup allows to identify the AB destruction mechanism of the FET. Usually, in the case of BJT latch-up, the FET semiconductor structure remains undamaged, since the setup circuit is designed to prevent an uncontrolled current rise even if control over the DUT is lost. On the contrary, in case of thermal breakdown, the DUT is destroyed inevitably. It should be noted that BJT latch-up occurs only in non-optimal FET structures. The possibility of this failure can be eliminated completely by optimizing the structure. In practice, thermal breakdown dominates. The BJT latch-up effect was not observed during IRF640 AB tests.

Since the thermal destruction mechanism is the dominant one, we examine it in more detail. Thermal destruction is induced by abrupt local heating of the reverse-biased $p-N$ junction of the built-in diode with its maximum operating temperature limited by intrinsic temperature T_i of the semiconductor at which the concentration of thermally generated carriers is equal to the concentration of the dopant impurity in the N^- layer. At room temperature, intrinsic carrier concentration n_i in silicon, $\sim 10^{10}\,\mathrm{cm}^{-3}$, is low compared to typical doping levels. However, n_i increases exponentially with temperature, and thermal generation becomes dominant at temperatures above T_i. The dependence of T_i on dopant concentration N is shown in Figure 4 [8,9]. During AB, the peak power dissipated at the $p-N$ junction may reach several tens of kW, which leads to a rapid local temperature rise. The increase in temperature of the diode $p-N$ junction is reflected in the oscillograms by an increase in the FET drain–source voltage. According to the model proposed by Selberherr [10], which is a variation of the classical avalanche breakdown model [11], the rate G of carrier generation due to impact ionization is equal to

$$G = \alpha_n J_n + \alpha_p J_p, \tag{3}$$

where J_n and J_p are the electron and hole current densities and α_n and α_p are the impact ionization coefficients, which depend on the electric field strength and temperature in the

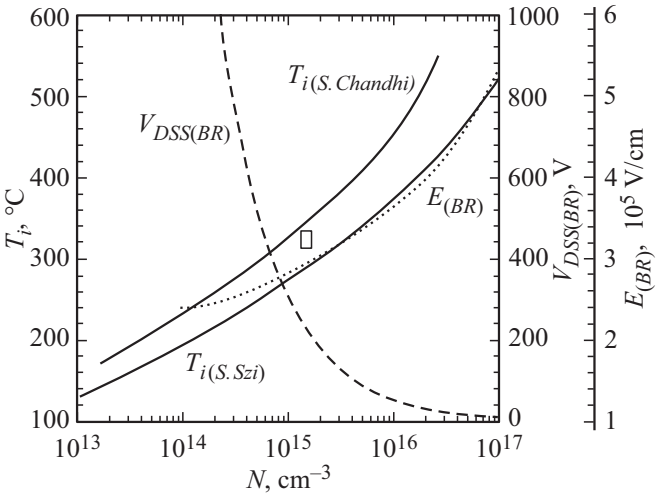

Figure 4. Intrinsic temperature T_i plotted according to [8,9] (solid curves), breakdown voltage $V_{DSS(BR)}$ (dashed curves), and breakdown electric field E_{BR} (dotted curve) as functions of N doping level in silicon. The rectangle in the figure marks the region (the range of calculated peak lattice temperatures, determined with account for technological deviations) where IRF640 thermal destruction occurs.

following way:

$$\alpha_n = 7.03 \cdot 10^5 \cdot \left(1 + 0.588 \cdot \left(\frac{T}{300} - 1\right)\right) \times \exp\left(-1.231 \cdot 10^6 \cdot \frac{1 + 0.248 \cdot (\frac{T}{300} - 1)}{E}\right), \quad (4)$$

$$\alpha_p = 6.71 \cdot 10^5 \cdot \left(1 + 0.588 \cdot \left(\frac{T}{300} - 1\right)\right) \times \exp\left(-1.693 \cdot 10^6 \cdot \frac{1 + 0.248 \cdot (\frac{T}{300} - 1)}{E}\right), \quad (5)$$

where T is the crystal lattice temperature in K.

It follows from (4) and (5) that α_n and α_p depend exponentially on E. When the E_{BR} threshold is exceeded, G increases sharply and AB occurs. However, since α_n and α_p decrease with increasing temperature, E_{BR} and $V_{DSS(BR)}$ have a positive temperature dependence. The growth of the drain–source voltage during AB clearly indicates an increase in the crystal lattice temperature T, which can be calculated by solving the inverse problem. The following algorithm is proposed for this purpose:

1. $V_{DSS(BR)}(T = 300\,\mathrm{K})$ is determined experimentally at a low avalanche breakdown energy (e. g., $V_{DSS(BR)}(T = 300\,\mathrm{K}) = 235\,\mathrm{V}$ at current $I_m = 1\,\mathrm{A}$ and an AB energy of 6.25 mJ in Figure 3).

2. It is assumed that the p–N junction of the built-in diode is sharp. The plots in Figure 4 [9] are used to estimate the doping level of the N^- layer and the breakdown electric field at 300 K $E_{BR}(T = 300\,\mathrm{K})$ (for IRF640: $N^- = 1.4 \cdot 10^{15}\,\mathrm{cm}^{-3}$, $E_{BR}(T = 300\,\mathrm{K}) = 2.92 \cdot 10^5\,\mathrm{V/cm}$).

3. The $V_{DSS(BR),\max}$ maximum value is determined from the oscillograms of DUT drain–source voltage (Figure 3), and $E_{BR}(T)$ can be calculated as follows:

$$E_{BR}(T) = E_{BR}(T = 300\,\mathrm{K}) \cdot \sqrt{\frac{V_{DSS(BR),\max}}{V_{DSS(BR)}(T = 300\,\mathrm{K})}}. \quad (6)$$

4. Now is possible to calculate T. To do this, we take into account the fact that carriers are generated in a narrow AB region near the p–N junction of the diode where the electric field strength is close to E_{BR}. Because its width is much smaller than that of the N^- layer, the 3-dimensional physical model can be reduced to a 1D one. The AB region is narrow, and the thermal conductivity of silicon is quite high (thermal diffusion coefficient is $\sim 1\,\mathrm{cm}^2/\mathrm{s}$). Therefore, thermal equilibrium in the AB region is established within ≤ 10 ns. Since the AB process lasts for tens and hundreds of μs (see Figure 3), it can be considered quasi-static, and assume that, at any given time T, α_n and α_p are the same at all points within the AB region. An electron-hole pair is produced as a result of each ionization event. Therefore, the increase in the number of electrons equals the increase in the number of holes at each point within the AB region. Electrons move towards the cathode of the diode under the influence of an electric field, while holes move towards the anode. Let us bear in mind that the saturated velocity v_{sat} of the electrons in silicon is close to that of the holes and, therefore, the following equations are correct at each point within the AB region:

$$dn/dx = -dp/dx \quad \text{and} \quad dJ_n/dx = -dJ_p/dx. \quad (7)$$

Outside the AB region, the conduction current J is exclusively electron current ($J = J_n|_{N^-}$) from the cathode side and exclusively hole current ($J = J_p|_{p^+}$) from the anode. Therefore, $J_n|_{N^-} = J_p|_{p^+} = J$. Note also that the current density in FETs during AB is relatively low: J is normally two–three orders of magnitude smaller than $J_{\mathrm{crit}} = eN^- v_{\mathrm{sat}}$. Therefore, the carrier density in a flux is significantly lower than the doping concentration and there is no significant field distortion by the moving carriers in the space charge region (SCR). $J = J_n + J_p$ in the AB region. The electron current density increases linearly towards the cathode from zero to J at the region boundary, and the hole current density increases similarly towards the anode. The number of electrons and holes generated per unit of time in the AB region with width w and area S is equal to

$$\begin{aligned}\int_0^w G(x)S dx &= S\int_0^w \Big(\alpha_n J_n(x) + \alpha_p J_p(x)\Big)dx \\ &= SJ\int_0^w \left(\frac{\alpha_n J_n(x)}{J} + \frac{\alpha_p J_p(x)}{J}\right)dx \\ &= SJ\int_0^w \left(\alpha_n \frac{x}{w} + \alpha_p\Big(1 - \frac{x}{w}\Big)\right)dx \\ &= SJ\left(\alpha_n \frac{x^2}{2w} + \alpha_p\Big(x - \frac{x^2}{2w}\Big)\right)\Bigg|_0^w \\ &= Sw\frac{J}{2}(\alpha_n + \alpha_p). \end{aligned} \quad (8)$$

The AB current through the FET operating on an inductive load is determined by the external circuit. The generation process provides the required number of carriers to maintain a given current and is self-stabilizing. That is, the negative temperature dependence of α_n and α_p parameters is compensated by a corresponding increasing E_{BR}:

$$\alpha_n(T) + \alpha_p(T) = \alpha_n(T = 300\,\mathrm{K}) + \alpha_p(T = 300\,\mathrm{K}). \quad (9)$$

Next, the inverse problem should be solved using the $E_{BR}(T = 300\,\mathrm{K})$ and $E_{BR}(T)$ values determined at stages 2 and 3, i. e. it is necessary to find the value of T that satisfies Eq. (9).

The proposed algorithm was used to find the critical temperature at which AB thermal destruction of IRF640 was observed. It is marked by a rectangle in Figure 4, which

indicates the range of calculated peak lattice temperatures, determined with account for technological deviations. The obtained values of critical temperature is in good agreement with the theoretical value of T_i.

The experimental results confirmed that the designed setup is efficient for testing the FET resistance to AB while they operate on an inductive load. Typical oscillograms of IRF640 drain–source voltage and current are shown in Figure 3. The transistor collapsed at a current of 16 A and an AB energy of 1.6 J (upper current and voltage curves in Figure 3). The moment of collapse is marked with a cross in Figure 3.

Thus, a detailed analysis of physical processes and mechanisms of FETs destruction during an avalanche breakdown was performed. In practice, thermal destruction of FETs mostly occurs when the lattice temperature near the $p-N$ junction of the built-in diode exceeds its intrinsic temperature T_i. A method for calculating the peak temperature of the crystal lattice during avalanche breakdown has been proposed. It is based on the analysis of FET drain–source voltage oscillograms. The calculated lattice temperature is in good agreement with the theoretical value of T_i and allows us to predict the threshold critical energy of the avalanche breakdown without physical destruction of the FET. A setup for testing the FETs resistance to avalanche breakdown while operating on an inductive load has been designed. The setup allows to test FETs at avalanche energies ranging from 0.5 mJ to 2.5 J and identify the possible mechanisms of FET destruction. The implemented circuit design allows testing both packaged field-effect transistors and chips on uncut semiconductor wafers. The manufactured setups were supplied to the production lines of semiconductor device factory, where they operate successfully.

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Conflict of interest

The authors declare that they have no conflict of interest.

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