Modeling of transport and emission characteristics of light-emitting lateral silicon p^+-i-n^+ transistor with self-assembled Ge(Si) nanoislands

© E.V. Demidov, V.E. Zakharov, V.B. Shmagin, A.N. Yablonskiy, A.V. Novikov

Institute of Physics of Microstructures, Russian Academy of Sciences,
603950 Nizhny Novgorod, Russia

E-mail: demidov@ipmras.ru, zakharov@ipmras.ru

Received June 4, 2025
Revised June 23, 2025
Accepted July 17, 2025

Presents the modeling of transport and radiation characteristics of previously experimentally studied light-emitting lateral silicon p^+-i-n^+ transistors with an array of self-assembled Ge(Si) nanoislands grown on a silicon on insulator substrate. The performed modeling made it possible to quantitatively explain experimental results indicating the possibility to control the spatial distribution of radiation intensity in such light-emitting transistors by applying a bias voltage to the substrate. It is shown that such a possibility arises due to the control of the conduction channel for electrons or holes formed at the boundary of the structure with a hidden oxide.

Keywords: light-emitting p^+-i-n^+ transistors, GeSi nanoislands, spatial localization, electroluminescence.

DOI: 10.61011/SC.2025.04.61724.8246

1. Introduction

Silicon photonics (SP) have been demonstrating a vigorous growth in recent years becoming one of the most promising areas in modern electronics. This is caused by a high degree of photonic and electronic component integration offering broad opportunities for developing various functional devices [1]. The main platform for formation of SP components currently consists of „silicon-on-insulator" (SOI) structures that are used to make all necessary component in the integrated form such as planar waveguides, modulators and dividers [2]. One of the key problem of the current SP development is the integration of high-performance light sources based on $A^{III}B^{V}$ direct-band materials both by bonding [3] and by heteroepitaxial growth on Si [4].

For obvious reasons, light sources directly on the basis of silicon are the most promising ones in terms of possible integration into SP. Low efficiency due to the indirect-band-gap nature of the bulk silicon band structure is the main hindrance for the practical use of light-emitting silicon structures. At the same time, some recent works demonstrated integrated Si light-emitting diodes (LEDs), efficiency of which is already sufficient for using in some SP applications [5–7], in particular, for express testing of the resulting photonic circuits. Lateral LEDs where differently doped regions are coplanar and current flows are parallel to the structure surface are the most promising ones in terms of possible integration onto a SOI platform [7]. This type of LEDs is similar in design to a field transistor that is the key component of modern integrated circuits. Moreover, lateral LED light may be easily brought into a planar waveguide formed on the same structure [7]. One of the considerable drawbacks of LEDs working on interband transitions in bulk Si is the strong absorption of light from such diodes in Si planar waveguides. Consequently, a distance, at which light of such LEDs may be conveyed through Si planar waveguides, is 200 μm max [7].

SiGe-heterostructure-based light sources working in the 1.3–1.55 μm region, i.e. in the bulk Si transmission region, are free of this drawback [8–10]. Sources based on self-assembled Ge(Si)/Si(001) nanoislands are most compatible with the SOI platform among such sources because thick buffer layer growth is not required for formation of such sources and they may be grown directly in SOI substrates [11]. Development of effective lateral $p-i-n$-LEDs on SOI structures with self-forming Ge(Si) nanoislands was reported recently [12]. High efficiency for Si-based light sources was achieved due to incorporation of a photonic crystal into the i-region of LED and, thus, the emitting power of islands was increased within 1.3–1.55 μm and values comparable with those for integrated Si-lateral LEDs were achieved [12]. In addition, inhomogeneous spatial distribution of electroluminescence (EL) intensity in the formed LEDs with a long base and controllability of this distribution by applying a control potential to the SOI substrate were demonstrated [13]. Therefore, the LEDs may be used as light emitting transistors to offer new opportunities for light control, in particular for control of spectral characteristics [13]. Note that the concept of forming lateral light emitting transistors is currently well developed primarily for organic semiconductor structures [14,15], while very few studies address implementation of such light sources on SOI structures [16].

In [13], an assumption was made that the identified inhomogeneous spatial distribution of the EL signal along the i-region of the prepared LEDs with Ge(Si) islands was associated with spatial localization of holes in the

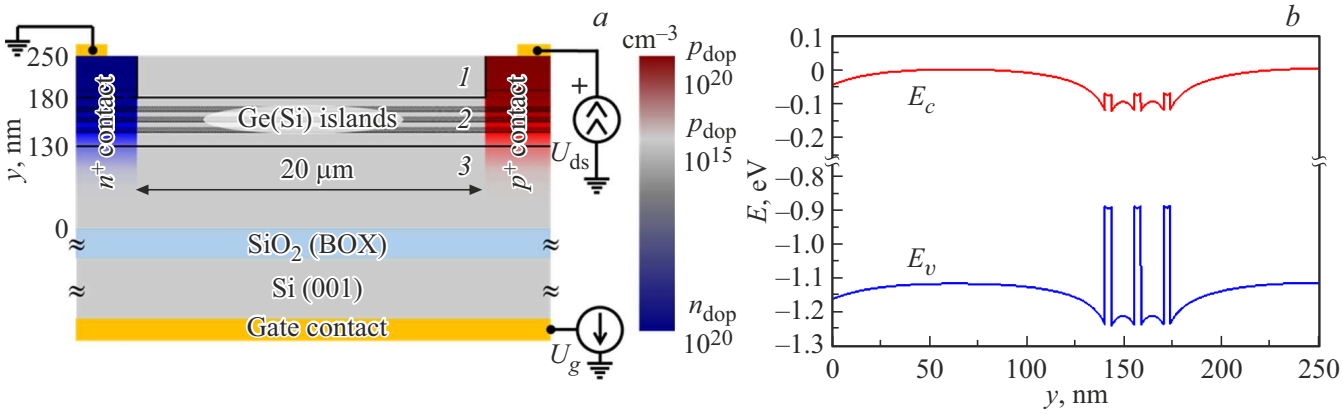

Figure 1. *a* — diagram of light emitting transistor with Ge(Si) islands used for the calculations. Numbers denote: *1* — coating Si layer; *2* — layer with Ge(Si) islands; *3* — buffer Si layer between the layer with islands and buried SiO_2-layer. Color scale shows the type and level of doping of various regions. The figure also shows the diagram of voltage supply to the structure. *b* — energy band diagram of the structure in the growth direction in the center of the *i*-region (10 μm from the contact regions) calculated at $I_{ds} = 0.5$ mA through the diode and bias of $U_g = 0$ B.

islands, and the dependence of this distribution on the magnitude and sign of potential applied to the substrate is associated with formation of a conductivity channel for particular type of charge carriers (electrons or holes) at the interface between silicon and buried oxide layer of the SOI substrate. This work describes numerical simulation of light emitting diodes and transistors experimentally studied in [12,13] to confirm this assumption. Band diagram of Ge(Si) islands was used to calculate spatial distributions of charge carriers and electroluminescence intensity depending on the control voltage on the substrate. Calculation data was compared with the experimental data reported in [12,13]. A mechanism responsible for the variation of spatial distribution of EL intensity in the prepared light emitting transistors during polarity inversion and change of the magnitude of the control voltage applied to the substrate is discussed.

2. Description of the model to be used

As shown above, transport and emitting properties of the previously formed p^+-i-n^+ LEDs and light-emitting transistors (LETs) with self-assembled Ge(Si) nanoislands were simulated in the work. Technique for forming such structures and experimental data are described in [12,13]. Diagram of the simulated transistor structures is shown in Figure 1, *a*. The structures were grown on a SOI substrate with a thick (2 μm) buried oxide (BOX) layer. The structures contained buffer and coating Si layers, between which lattice of 3 to 5 Ge(Si) nanoisland layers separated by 15 nm Si layers was formed. The total thickness of the structure above the oxide layer was ~ 250 nm. Conductivity type of the *i*-region of diodes was defined by residual acceptors ($N_a = 10^{15}-10^{16}$ cm^{-3}). According to the results of previous studies [17], boron and phosphorus concentration in doped contact *p*- and *n*-regions, respectively, was $10^{18}-10^{20}$ cm^{-3}. The length of the *i*-region (distance between the n^+- and p^+-contact regions) of the LEDs and LETs addressed in this paper was 20 μm.

Numerical simulation of LEDs was performed using Comsol Multiphysics software package within a two-dimensional model (Figure 1, *a*). Simulation involved the calculation of spatial distributions of charge carriers, currents and EL intensity. For this, self-consistent solution of the two-dimensional Poisson equation was found taking into account electron and hole distribution. Diffusion-drift approximation was used to describe charge carrier transport. The nonradiative Shockley–Read–Hall recombination was taken into account for the charge carrier distribution simulation. Due to indirect type of band configuration in the given structures, radiative recombination was expected to have low influence on charge carrier distribution. For the purpose of calculation, concentration of residual acceptors in the *i*-region was assumed equal to $N_a = 3 \cdot 10^{15}$ cm^{-3} (Figure 1, *a*). Distributions of electron and hole concentrations over the structure thickness in the contact n^+- and p^+-regions corresponded to experimental dopant distributions in these regions [17].

Model calculations were performed for diodes containing three Ge(Si) island layers separated by 15 nm Si layers (Figure 1). Layers with islands were at 130–180 nm from the Si-BOX interface (Figure 1), which corresponded to island location in the experimentally studied structures [12,13]. For the purpose of simulation, island sizes were set to 90 nm in the growth plane and to 7 nm in the vertical direction, which corresponded to the size of islands in LEDs formed at the growth temperature of 600 °C [18]. Islands were assumed to have a form of truncated pyramid, which is close to the real form of buried Ge(Si) islands in the given structures [18]. It is known that Ge(Si) islands are a deep potential well for holes [19] (Figure 1, *b*). For the purpose of calculations, the potential well depth was set to 0.3 eV, which is a typical

value for Ge(Si) islands grown at 600 °C [20]. In the absence of current due to type II band discontinuity, a small barrier for electrons is formed for the Ge-Si heteropair in the conduction band of the islands [19]. Potential well for electrons is formed in silicon layers at type II heterointerface, first, due to the strain in these layers near the island boundary due to a partial relaxation of elastic stresses in the islands and, second, due to the Coulomb potential of holes localized in the islands [19] (Figure 1, *b*). For the purpose of calculations, the potential well depth for electrons associated with the strain in the Si layers (without considering the Coulomb potential of holes) was assumed equal to 40 meV. As shown below, current flow through the diode affects considerably the magnitude of potential barriers in the structure conduction band.

The presence of potential barriers in islands and in their neighborhood affects considerably the charge carrier transport. Therefore, the *i*-region of simulated diodes was divided into three layers in thickness (Figure 1, *a*): cap Si (layer 1) layer containing a lattice with islands (layer 2) and Si layer between islands and BOX (layer 3).

For simulation of the transport properties of silicon layers (layers 1 and 3), an expression depending on doping level was used for mobility of electrons and holes in bulk silicon [21]:

$$\mu(N) = \mu_0 / \sqrt{1 + 1/(a + N_0/N)}, \qquad (1)$$

where for electrons $\mu_0 = 1450\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$, $a = 0.001$, $N_0 = 3 \cdot 10^{16}\,\mathrm{cm}^{-3}$, and for holes $\mu_0 = 470\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$, $a = 0.0123$, $N_0 = 4 \cdot 10^{16}\,\mathrm{cm}^{-3}$.

Dependence of electron and hole lifetime on the concentration of charge carriers in silicon was considered using the following expression [22]

$$\tau(N) = \tau_0/(1 + N/N_0), \qquad (2)$$

where $N_0 = 5 \cdot 10^{16}\,\mathrm{cm}^{-3}$. τ_0 served as one of the fitting parameters.

Simulation of the transport properties of the layer with Ge(Si)-islands is complicated by the fact that details of current transport between islands at microscopic level are not available. It is known that the deep potential well for holes in islands leads to the hopping type of hole conductivity in the layer with islands [23]. While electrons in the Si layers adjacent to islands are scattered at the potential barriers formed by Ge(Si) islands. Both factors lead to a considerable decrease in charge carrier mobility compared with bulk materials. Therefore, mobilities of electrons and holes in the GeSi layer served as fitting parameters. Simulation also considered series resistance of contact regions of the structure.

Due to type II band discontinuity in the structures with Ge(Si) islands, the main contribution to the luminescence signal of such structures is made by real-space indirect radiative recombination of holes localized in islands and electrons localized in Si layers at the island heterointerface [19,20]. However, as shown in Figure 1, *b*, at high hole injection levels, a small potential well for electrons may be also formed inside the islands. In this case, space-direct radiative recombination of electrons and holes in islands may also contribute to the luminescence of Ge(Si) islands. Therefore, the simulation assumed that the EL signal intensity of the Ge(Si) islands is proportional to the product of the concentration of holes localized in islands and the concentration of electrons localized both in islands and in the Si layer with islands (layer 2 in Figure 1, *a*). Since the charge carrier injection level and the radiation intensity in the studied LEDs are proportional to the current [12], the constant current mode $I_{ds} = 0.5\,\mathrm{mA}$ was used for comparison with the experimental data in calculations.

As shown earlier [13], formation of photonic crystals in light emitting transistors with Ge(Si) islands has no considerable effect on spatial distribution of island radiation intensity. Therefore, for simplicity, lateral light emitting diodes and transistors with Ge(Si) islands not containing photonic crystals were simulated in this work.

3. Results and discussion

Fitting parameters (series resistance of contact regions, charge carrier mobility in the layer with Ge(Si) islands, charge carrier lifetimes in the simulated structure) were determined by means of fitting to the experimental data of the calculated dependence of voltage drop between the source and drain regions of LET (U_{ds}) on the sign and magnitude of the control voltage on the substrate (U_g) with fixed current through the transistor (I_{ds}) (Figure 2). The calculations showed that holes were localized in the Ge(Si) islands that served as a deep potential well for them. Therefore, the hole mobility has a low effect on hole distribution and transport properties of LET. In further calculations, hole mobility in the layer with islands was assumed equal to $\mu_p = 50\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$. The qualitative form of $U_{ds}(U_g)_{I_{ds}=\mathrm{const}}$ is most affected by the electron mobility in the layer with Ge(Si) islands and by charge carrier lifetimes. For quantitative agreement with experimental data, the sign and charge density at the Si-BOX interface were also considered.

As was experimentally shown before [13], control voltage applied to the structure's substrate affects considerably the LET conductivity (Figure 2). According to the simulation (Figures 3 and 4), this is caused by two main current flow channels in the studied diodes: integrated channel — on the layer with Ge(Si) islands and induced layer — at the Si-BOX interface. Relation of contributions of these channels to the total transistor conductivity depends heavily on the sign and magnitude of the control voltage on the substrate. Low conductivity of the cap Si layer (layer 1 in Figure 1, *a*) and of the most part of the buffer Si layer (layer 3 in Figure 1, *a*) is attributable to the spatial localization of injected holes in Ge(Si) islands. Accumulation of holes in islands leads to the occurrence

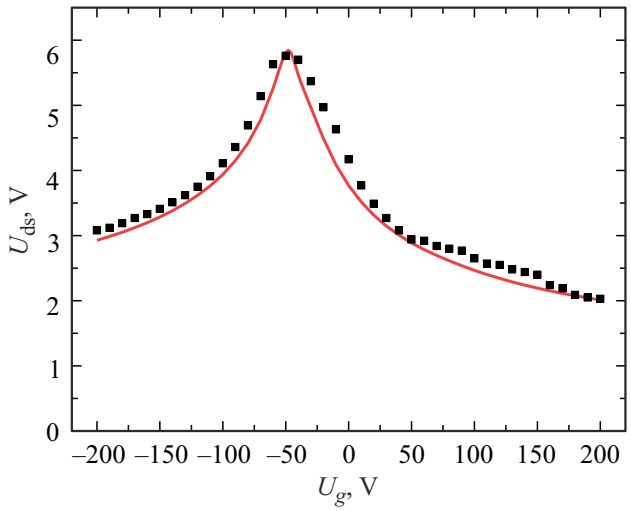

Figure 2. Comparison of the experimental (symbols) and calculated (solid line) dependences of the voltage between the LET source and drain (U_{ds}) on the gate voltage (U_g) in the set source–drain current mode ($I_{ds} = 0.5$ mA).

of the Coulomb potential that considerably modifies the energy band positions in the layer with Ge(Si) islands (Figure 1, *b*). The presence of this potential leads to an increase in the potential well depth for electrons in Si layers in the vicinity of islands (layer 2 in Figure 1, *a*) and to the occurrence of a potential well for electrons directly in islands (Figure 1, *b*). Electrons ultimately also get to be localized in the layer with islands, though their localization potential is still much lower than for holes (Figure 1, *b*). Due to the presence of potential barriers both for holes and electrons, conductivity of the layer with Ge(Si) islands turns out to be quite low. Therefore, the maximum value of U_{ds} in $U_{ds}(U_g)_{I_{ds}=\text{const}}$ is expected to be observed if there is the lowest contribution of the induced channel at the Si-BOX interface to the LET conductivity. Calculations showed that, when a built-in surface charge is not available at the Si-BOX interface, this maximum shall be observed at a low negative voltage $U_g \approx -15$ V, rather than at zero voltage on the substrate ($U_g = 0$ V). This is attributable to the difference in hole and electron mobilities in silicon, and to the aspects of flow of charge carriers with unlike signs through the diode structures of interest. However, the maximum on the experimental $U_{ds}(U_g)_{I_{ds}=\text{const}}$ is observed at higher negative control voltages ($U_g \approx -50$ V) (Figure 2). This indicates that there is a built-in positive charge at the Si-BOX interface, and this charge causes the formation of a conductivity channel for electrons at this interface, when there is no control voltage (Figure 4). Application of positive control voltage to the substrate increases the conductivity of this channel (Figure 4) and, therefore, the total transistor conductivity (Figure 2).

When a low negative control voltage is applied to the substrate, the conductivity channel for electrons at the Si-BOX interface disappears and the transistor conductivity decreases. According to the calculations, the experimentally observed maximum on $U_{ds}(U_g)_{I_{ds}=\text{const}}$ at $U_g \approx -50$ V (Figure 2) indicates that there is a positive charge at the Si-BOX interface with the surface density $N_s = 3.5 \cdot 10^{11}$ cm^{-2}. At higher negative control voltages, a conductivity channel for holes is formed at the Si-BOX interface (Figure 3), which, as with the positive control voltages, causes an increase in the total transistor conductivity and a decrease in voltage drop between the source and drain at fixed I_{ds} (Figure 2). But at $U_g < -50$ V, the conductivity increases due to an increase in the contribution of the hole component of current to the conductivity resulting from formation of the conductivity channel for holes at the Si-BOX interface (Figure 3).

The calculations showed that the best agreement between the calculated and measured $U_{ds}(U_g)_{I_{ds}=\text{const}}$ is achieved at the following fitting parameters: series resistance of contact regions — 600 Ohm; charge carrier lifetime $\tau_0 = 2.5 \cdot 10^{-9}$ s; electron and hole mobility in the region with Ge(Si) islands $\mu = 50$ cm^2/(V·s); surface density of the positive charge at the Si-BOX interface $N_s = 3.5 \cdot 10^{11}$ cm^{-2}. The fitting parameters listed above provide good quantitative description of the experimental dependence of the LET transport properties on the magnitude and sign of U_g across the entire variation range (Figure 2). Note that high control voltages on the substrate needed for observing the above-mentioned effects are associated with large ($2\,\mu$m) thickness of the buried oxide layer in the devices of interest. Low value of τ_0 is attributable to the nonradiative carrier recombination at the structure interfaces (surface and Si-BOX interface), and at point defects in the structure itself.

The calculated carrier concentration distributions in the simulated LETs and their dependence on the substrate control voltage are used to evaluate the radiative recombination intensity in the simulated devices, spatial distribution of the radiative recombination and the influence of the substrate potential on this distribution. Since the electroluminescence intensity is defined by the radiative recombination intensity of charge carriers in the structure, the calculation data may be compared with the experimental data obtained in [13].

The calculations show (Figures 1, *b*, 3 and 4) that, when current passes through LET, electrons and holes turn out to be localized in the layer with islands. High concentration of one of the charge carrier types may be also observed near the Si-BOX interface in the conductivity channel for electrons or holes (depending on the control voltage sign and magnitude) being formed at this interface (Figures 3 and 4). In the specified induced conductivity channel, unlike the layer with Ge(Si) islands, increase in the concentration of one charge carrier type is accompanied with the drop of concentration of the other carrier type (Figures 3 and 4) leading to low radiative recombination intensity in this region at any control voltages. As a result, according to the calculations, the EL intensity associated with the charge carrier recombination in the layer with Ge(Si) islands shall be much higher than the interband EL intensity in Si layers

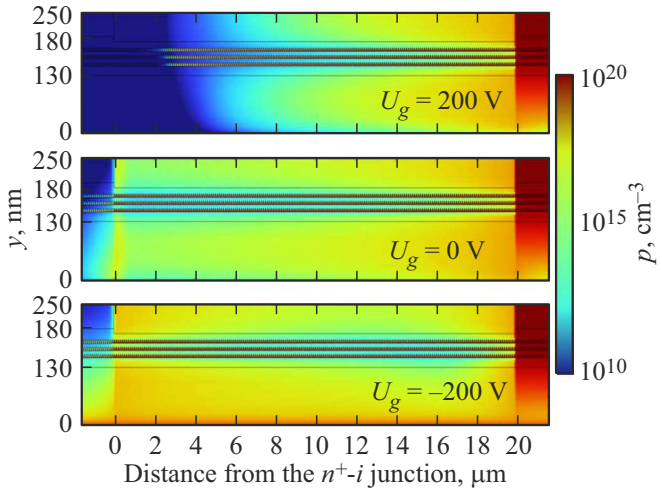

Figure 3. Calculated hole concentration distributions in the LET structure of interest for three values of U_g at $I_{ds} = 0.5$ mA. Zero value on the y axis corresponds to the Si-BOX interface.

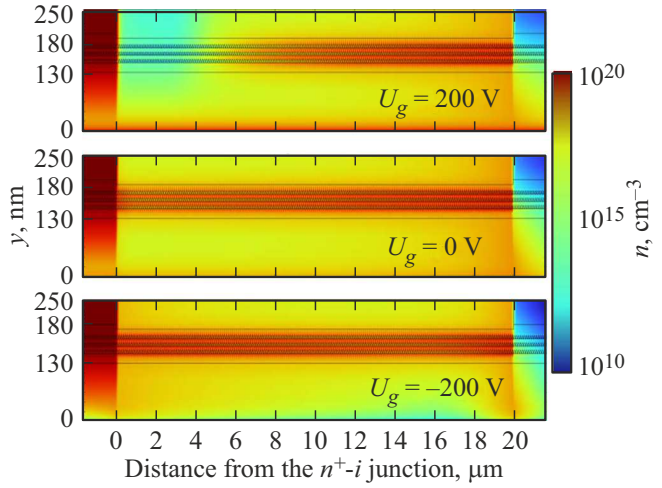

Figure 4. Calculated electron concentration distributions in the LET structure of interest for three values of U_g at $I_{ds} = 0.5$ mA. Zero value on the y axis corresponds to the Si-BOX interface.

of the LEDs and LETs of interest, and it is just the case that is observed experimentally [12,13]. Consequently, the radiative properties of LETs are governed primarily by the charge carrier (electrons and holes) concentration in the layer with Ge(Si) islands, concentration distribution along the diode and dependence on the substrate (gate) control voltage.

As shown above, distribution and transport of electrons and holes in the layer with Ge(Si) islands are significantly affected by the island potential, owing to which a deep potential well for holes is formed in islands. Potential well for electrons in the layer with Ge(Si) islands have a smaller depth, therefore, the spatial distribution of EL intensity in the simulated LETs is assumed to be primarily defined by the hole concentration distribution in the layer with Ge(Si) islands. Figure 5, *a* shows the calculated distributions of the numbers of holes localized in each Ge(Si) island along the length of the *i*-region of the given structure at three different values of U_g. According to the calculations, the total (over the layer thickness) concentration of electrons (located both in Si and in islands) in the layer with Ge(Si) islands (layer 2 in Figure 1, *a*) follows the distribution of the number of holes in islands due to the principle of electroneutrality.

It follows from the above-mentioned simulation of the LET transport properties that Ge(Si) islands may be filled with holes either directly by means of injection from the contact p^+-region or as a result of hole diffusion from the conducting channel at the Si-BOX interface (at $U_g < -50$ V). At $U_g \geq -50$ V, Ge(Si) islands are filled with holes only through hole injection from the p^+-contact directly into the layer with islands (Figure 3). Due to hole capture into islands and effective hole localization, hole concentration in the layer with islands decreases quickly with distance from the p^+-contact, and the maximum number of holes in islands is observed at the $i-p^+$ junction (Figure 5, *a*). Therefore, at $U_g \geq -50$ V, the EL intensity near the p^+-contact is much higher than near the n^+-contact both in the experiment and in the calculation data (Figure 5, *b*). For the simulated LETs with the positive charge density at the Si-BOX interface of $N_s = 3.5 \cdot 10^{11}$ cm^{-2} at fixed $I_{ds} = 0.5$ mA, the maximum EL intensity near the p^+ contact is observed at low negative gate voltages (Figure 5, *b*). However, note that LET has low conductivity at such control voltages (Figure 2), i.e. its efficiency as a light source will be low at this control voltage. Decrease in the EL intensity near the p^+-contact at high positive values of U_g (Figure 5, *b*) is associated with the increase in the potential barrier for holes at the $i-p^+$ junction, leading to a decrease in the hole injection into the *i*-region.

At high negative control voltages ($U_g < -50$ V) at the Si-BOX interface, the hole conductivity channel is formed. As shown above, Ge(Si) islands may be filled with holes in these conditions both through direct hole injection into the layer with islands from the p^+-contact and through hole diffusion from the conducting channel to islands. Since the motion of holes along the conductivity channel in the vicinity of the Si-BOX interface is not hindered by the processes of capture in Ge(Si) islands (due to the absence of islands in this structure region), filling of islands with holes through diffusion from the conductivity channel may occur along the full length of the *i*-region from the p^+-contact to the n^+-contact (Figures 3 and 5, *a*). The calculation data shows that this process is implemented most effectively in the vicinity of the n^+-contact because islands in this region are filled with holes from the conductivity channel both through hole diffusion under the action of the concentration gradient (that weakly varies along the channel length) and through the enhancement of the drift component of the hole current (under the field action) from the channel into the layer with islands. Consequently, besides the maximum distribution of the number of holes in islands and,

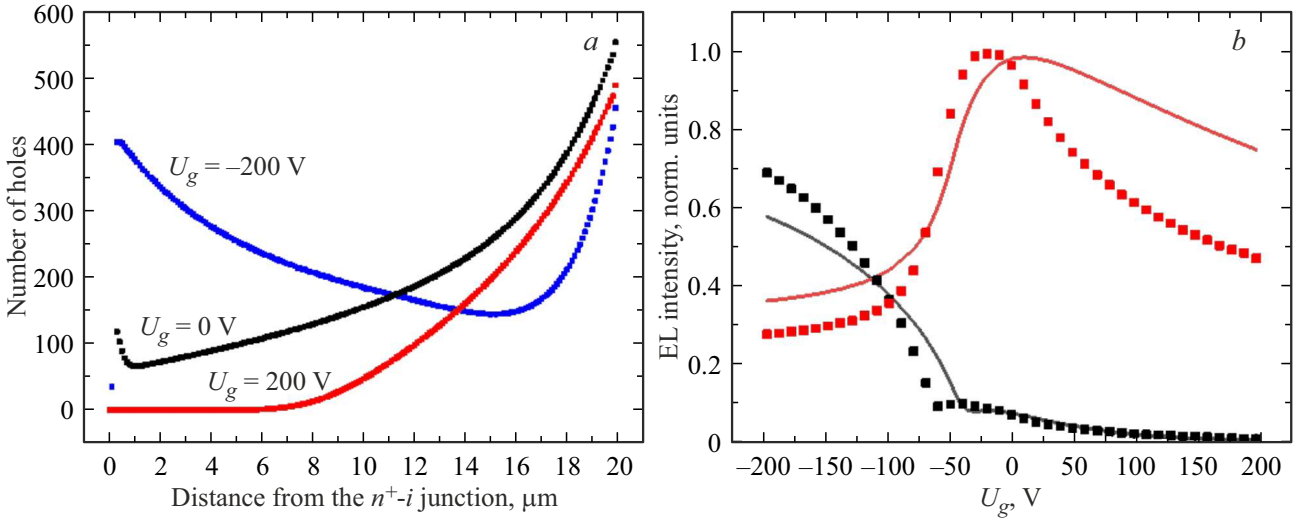

Figure 5. *a* — calculated spatial hole distributions in the layer with Ge(Si) islands along the *i*-region of LET for three different values of U_g. The number of holes per Ge(Si) island is plotted on the vertical axis. *b* — experimentally measured (symbols) and simulated (solid lines) dependences of the EL intensity at the „n^+-i“ (black symbols and black solid curve) and „p^+-i“ (red symbols and red solid curve) junctions on the sign and magnitude of U_g. Measurements and calculations were performed for $I_{ds} = 0.5$ mA.

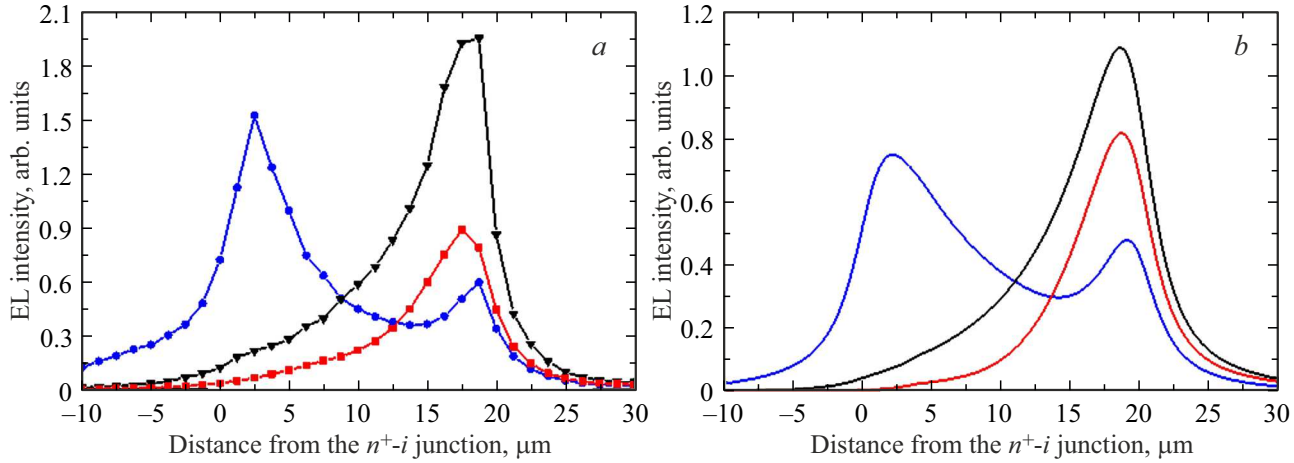

Figure 6. Experimentally measured (*a*) and calculated (*b*) spatial distributions of the EL intensity along LET for $U_g = 0$ V (black curves), $U_g = 200$ V (red curves) and $U_g = -200$ V (blue curves). Measurements and calculations were performed for $I_{ds} = 0.5$ mA.

accordingly, of the EL intensity near the p^+-contact (that is observed at any control voltages), additional maximum occurs at $U_g = -200$ V in the vicinity of the n^+-contact (Figure 5, *a*, *b*).

Thus, the calculations provide a good quantitative description of the experimental dependences of the EL intensity at the junction between the *i*-region and contact regions from the substrate control voltages (Figure 5, *b*). They also allow qualitative reproduction of experimentally measured spatial distributions of the EL intensity along LET for various control voltages (Figure 6). As described above, at $U_g \geq 0$ V, the EL signal maximum is observed only near the p^+-contact (Figure 6). At the same time, at high negative values of U_g, EL signal maxima are observed in the vicinity of both contact regions, with the maximum at the n^+-contact characterized by higher intensity (blue curves in Figure 6). High EL intensity near heavily doped regions is typical of various $p-i-n$-LEDs and is defined by high charge carrier concentration in these regions.

4. Conclusion

The study develops a two-dimensional model to describe transport and luminescent properties of lateral light emitting p^+-i-n^+-transistors made on the basis of Si structures with self-assembled Ge(Si) islands grown on the SOI substrate. Considering the spatial localization of holes in Ge(Si) islands and electrons in the vicinity of islands, and the presence of charge at the interface between the structure and buried oxide, main properties of similar light

sources experimentally studied in previous works [12,13] were described quantitatively. In particular, the influence of the magnitude and sign of the control voltage applied to the SOI substrate on the general EL signal intensity and spatial distribution of EL intensity along the i-region of the transistor matches well with formation of the induced conductivity channel for electrons and holes at the interface between the structure and buried oxide layer. Experimentally observed maximum EL intensity near the contact p^+-region in the absence of gate control voltage is attributable to the effective localization of holes injected into the i-region of diodes in Ge(Si) islands. The developed model may be used to find the ways to increase the efficiency of Si-based light sources and enhance the opportunities to control their radiative properties.

Funding

The study was funded by the Russian Science Foundation (grant No. 25-12-00367).

Conflict of interest

The authors declare no conflict of interest.

References

[1] S. Shekhar, W. Bogaerts, L. Chrostowski, J.E. Bowers, M. Hochberg, R. Soref, B.J. Shastri. Nature Commun., **15**, 751 (2024). https://doi.org/10.1038/s41467-024-44750-0
[2] S.Y. Siew, B. Li, F. Gao, H.Y. Zheng, W. Zhang, P. Guo, S.W. Xie, A. Song, B. Dong, L.W. Luo, C. Li, X. Luo, G.-Q. Lo. J. Lightwave Technol., **39**, 4374 (2021). https://doi.org/10.1109/JLT.2021.3066203
[3] S.Y. Bao, Y. Wang, K. Lina, L. Zhang, B. Wang, W.A. Sasangka, K.E.K. Lee, S.J. Chua, J. Michel, E. Fitzgerald, C.S. Tan, K.H. Lee. J. Semicond., **42** (2), 023106 (2021). https://doi.org/10.1088/1674-4926/42/2/023106
[4] Y. Hu, D. Liang, K. Mukherjee, Y. Li, C. Zhang, G. Kurczveil, X. Huang, R.G. Beausoleil. Light: Sci. Appl., **8**, 93 (2019). https://doi.org/10.1038/s41377-019-0202-6
[5] Z. Li, J. Xue, M. Cea, J. Kim, H. Nong, D. Chong, K.Y. Lim, E. Quek, R.J. Ram. Nature Commun., **14**, 882 (2023). https://doi.org/10.1038/s41467-023-36639-1
[6] J. Xue, J. Kim, A. Mestre, K.M. Tan, D. Chong, S. Roy. IEEE Trans. Electron Dev., **68** (8), 3870 (2021). https://doi.org/10.1109/TED.2021.3085541
[7] M. Cea, Z. Li, M. Notaros, J. Notaros, R.J. Ram. APL Photonics, **8**, 081301 (2023). https://doi.org/10.1063/5.0156602
[8] J. Liu, X. Sun, R. Camacho-Aguilera, L.C. Kimerling, J. Michel. Optics Lett., **35** (5), 679 (2010). https://doi.org/10.1364/OL.35.000679
[9] X. Xu, T. Tsuboi, T. Chiba, N. Usami, T. Maruizumi, Y. Shiraki. Opt. Express, **20**, 14714 (2012). https://doi.org/10.1364/OE.20.014714
[10] R. Koerner, M. Oehme, M. Gollhofer, M. Schmid, K. Kostecki, S. Bechler, D. Widmann, E. Kasper, J. Schulze. Opt. Express, **23** (11), 14815 (2015). https://doi.org/10.1364/OE.23.014815
[11] M. Brehm, M. Grydlik. Nanotechnology, **28**, 392001 (2017). https://doi.org/10.1088/1361-6528/aa8143
[12] V.B. Shmagin, A.N. Yablonskiy, M.V. Stepikhova, D.V. Yurasov, A.N. Mikhaylov, D.I. Tetelbaum, E.E. Rodyakina, E.E. Morozova, D.V. Shengurov, S.A. Kraev, P.A. Yunin, A.I. Belov, A.V. Novikov. Nanotechnology, **35** (16), 165203 (2024). http://dx.doi.org/10.1088/1361-6528/ad1f8a
[13] A.N. Yablonskiy, V.B. Shmagin, V.E. Zakharov, D.V. Yurasov, M.V. Shaleev, E.V. Demidov, A.N. Mikhaylov, D.I. Tetelbaum, E.E. Rodyakina, E.E. Morozova, D.V. Shengurov, S.A. Kraev, A.V. Novikov. Appl. Phys. Lett., **125**, 231103 (2024). http://dx.doi.org/10.1063/5.0239609
[14] T. Oyamada, H. Uchiuzou, S. Akiyama, Y. Oku, N. Shimoji, K. Matsushige, H. Sasabe, C. Adachi. J. Appl. Phys., **98** (7), 074506 (2005). http://dx.doi.org/10.1063/1.2060932
[15] J. Zaumseil, R.H. Friend, H. Sirringhaus. Nature Materials, **5**, 69 (2006). https://doi.org/10.1038/nmat1537
[16] S. Saito, D. Hisamoto, H. Shimizu, H. Hamamura, R. Tsuchiya, Y. Matsui, T. Mine, T. Arai, N. Sugii, K. Torii, S. Kimura, T. Onai. Appl. Phys. Lett., **89** (16), 163504 (2006). https://doi.org/10.1063/1.2360783
[17] P.A. Yunnin, M.N. Drozdov, A.V. Novikov, V.B. Shmagin, E.V. Demidov, A.N. Mikhailov, D.I. Tetelbaum, A.I. Belov. Poverkhnost. Rentgenovskie, sinkhrotronnye i nejtronnye issledovaniya, № 5, 92 (2024). (in Russian). https://doi.org/10.31857/S1028096024050094
[18] Z.F. Krasilnik, A.V. Novikov, D.N. Lobanov, K.E. Kudryavtsev, A.V. Antonov, S.V. Obolenskiy, N.D. Zakharov, P. Werner. Semicond. Sci. Technol., **26**, 014029 (2011). https://doi.org/10.1088/0268-1242/26/1/014029
[19] V.Ya. Aleshkin, N.A. Bekin, N.G. Kalugin, Z.F. Krasilnik, A.V. Novikov, V.V. Postnikov, H. Seiringer. Pis'ma ZhTF, **67** 1, 46 (1998). (in Russian).
[20] N.V. Vostokov, Y.N. Drozdov, Z.F. Krasilnik, D.N. Lobanov, A.V. Novikov, A.N. Yablonsky. ZhETF **76**, (6), 425 (2002). (in Russian).
[21] D.L. Scharfetter, H.K. Gummel. IEEE Trans. Electron Dev., **16** (1), 64 (1969). https://doi.org/10.1109/T-ED.1969.16566
[22] D.J. Roulston, N.D. Arora, S.G. Chamberlain. IEEE Trans. Electron Dev., **29** (2), 284 (1982). https://doi.org/10.1109/T-ED.1982.20698
[23] N.P. Stepina, A.V. Nenashev, A.V. Dvurechenskii. JETP Lett., **106**, 308 (2017). http://dx.doi.org/10.1134/S0021364017170118

Translated by E.Ilinskaya