Control of charge carrier density in photo-FET structures based on atomically thin CVD-MoS_2

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Optimization of two-dimensional semiconductor properties for various electronic applications is one of the critical tasks facing the modern nanoelectronics. In this paper, the features of controlling the concentration of charge carriers in monolayer and bilayer MoS_2 by changing the gate voltage of the transistor are investigated. The influence of MoS_2 inclusions of two-layer thickness with regular ($3R$) and irregular stacking on the degree of nonlinearity of the current-voltage characteristics and the response of the MoS_2 parameters to the gate voltage is investigated.

Keywords: molybdenum disulfide, phototransistor, hysteresis, Raman spectroscopy, photoluminescence, charge carriers.

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1. Introduction

Two-dimensional semiconductors, including transition metal dichalcogenides (TMDs) have been used in the recent decade to create a full set of components for electrical circuits, for example, memristors — critical components for neuromorphic electrical circuits [1,2]. „Photodetector-field-effect transistor" (photo-FET) hybrid structures are a promising platform for developing next-generation optoelectronic devices. High sensitivity and increased signal-to-noise ratio achieved through dark current reduction with an increase in the intrinsic channel resistance during channel closure are the key advantages of these structures compared with the diode ones [3]. The use of two-dimensional semiconductors as a photosensitive channel allows for a significant reduction in both the size of devices and their power consumption. Molybdenum disulfide (MoS_2), one of the TMD family representatives, has high specific photosensitivity [4] and quite high carrier mobility [5], making it one of the most suitable materials for such devices.

Chemical vapor deposition (CVD) is the most common method of two-dimensional layer synthesis. However, due to the misalignment between the lattice parameters and substrate, island growth of MoS_2 takes place: crystallites with arbitrary oriented a and b axes lying in the layer plane are formed from randomly distributed nuclei [6]. This leads to high density of interdomain boundaries that act as nonradiative recombination and scattering centers and reduce the carrier concentration and mobility. However, the presence of structural defects may be useful for utilization of such films in some specific areas. Capture of charge carriers in traps associated with MoS_2 film defects may induce nonlinearity and hysteresis in current-voltage (I-V) characteristics of devices based on such films. The hysteresis-induced effect whereby a device's resistance depends on the time integral of the past current — also called the memristive effect — was first proposed in 1971 [7] and has since formed the basis of operation of a new class of electronic components: memristors. An important precondition for operation of such components is that the hysteresis loop passes through the origin of coordinates of the I-V curve [8], in contrast to ferroelectric or magnetic hysteresis.

Early memristors were based on oxide films, such as one of the first memristors based on TiO_2 thin film [9]. However, for a significant memristor effect to occur, a large active region area is required in such structures, which limits their scalability. A breakthrough in miniaturization became possible due to advancements in technologies concerning a group of two-dimensional materials. Use of two-dimensional semiconductors such as MoS_2 allows one to add a gate for additional channel resistance and hysteresis modulation, and to create a memtransistor [10].

Carrier density control in the phototransistor channel allows the photodetector sensitivity to be adjusted. In this case, the presence of defects and charge traps in the channel may affect the adjustment capability and range. Defects may include classical grain boundaries and vacancies as well as MoS_2 inclusions with different number of layers, and twisted stacking sequence regions. Polytypes $2H$ and $3R$ (space groups $P6_3/mmc$ and $R3m$, respectively) are the most common structural modifications of MoS_2. However, island growth provides conditions for possible build-up of the edge of one island over another [6] and formation of two-layer MoS_2 with twisted stacking sequence at the boundaries.

This work demonstrates the controllability of carrier concentration in the channel of transistors made of CVD-MoS_2. Changes are tracked using a combination of two optical techniques: Raman spectroscopy and photoluminescence (PL). Using Raman and PL transistor channel mapping, these techniques provide complementary information concerning not only carrier concentration changes, but also structural features of a particular transistor channel region, including the layer stacking sequence in multilayer regions. In this way, it is possible to investigate the features of the response to gate voltage of various regions of the MoS_2 phototransistor channel and to identify the regions making the main contribution to hysteresis.

MoS_2 was deposited on p^+-Si/SiO_2 wafers that were cleaned and cut into chips, and then treated in oxygen plasma during 10 min at 300 W power. After the plasma treatment, KCl was deposited from 0.05 M water solution by spin coating. Then, the MoS_2 crystal film was grown in a quartz tube using atmospheric pressure chemical vapor deposition (APCVD) with highly-oriented pyrolytic graphite (HOPG). Sigma-Aldrich's (S) and $(MoO)_3$ powders were used as precursors, and nitrogen was used as carrier gas. 800 °C in the MoO_3 source and wafer zone was reached within 18 min and maintained for 2 min. Then the chamber self-cooled to room temperature.

Transistor channels were formed from the deposited MoS_2 layer by reactive ion etching through the AZ 1518 photoresist used as a mask. Electrical contacts were made using the MLA 150 maskless lithography system (Heidelberg Instruments). AZ LNR-003 negative photoresist was used as a mask for metal deposition. A 100 nm golden film for contacts and bonding pads was deposited by electron beam vapor deposition using the CS400ES system (Ardenne).

Raman and PL spectra were measured using the Horiba LabRAM HREvo UV-VIS-NIR-Open spectrometer. The spectra were measured in backscattering geometry with continuous excitation by Nd:YAG laser (Laser Quantum Torus) with a wavelength of 532 nm and a power up to 400 μW. All optical measurements were performed at room temperature. Olympus LMPFLN100× (NA = 0.8) long-working-distance lens was used for laser beam focusing into an area $< 1\,\mu$m in diameter and PL and Raman signal acquisition from this region. Raman spectra were measured with a spectral resolution of 0.7 cm^{-1} using a 1800 grooves/mm grating and the Symphony BIUV detector (Horiba). PL spectra were measured using a 600 grooves/mm grating and the Synapse EMCCD detector (Horiba). Information about the ultra-low frequency range ($5-50\,cm^{-1}$) was obtained using a set of Bragg filters (BragGrate).

Raman and PL mapping measurements were conducted to examine the influence of gate voltage on the properties of various regions in the photo-FET channel. For measurements, the samples were placed into the Linkam HFS600-PB4 optical cell equipped with Au-coated tungsten probes. Voltage was applied to corresponding contacts of transistor structures using the Keysight B2900 source/measure unit.

In this work, two photo-FETs with different properties formed on a single chip were used: device 1 with the channel consisting predominantly of monolayer MoS_2 with a small fraction of bilayer inclusions and device 2 with a significant fraction of bilayer MoS_2 in the channel. MoS_2 thickness in the channel was measured by Raman mapping.

Figure 1 shows the I-V curves measured on both devices. For a memtransistor, hysteresis can be present both on the output and transfer I-V curves. The presence or absence of hysteresis in each particular case is defined by the localization of carrier traps in these components [11]. Thus, CVD-MoS_2-based memtransistors grown on Si/SiO_2 wafers feature carrier traps at the SiO_2/MoS_2 interface and traps associated with defects in the MoS_2 layer itself (S vacancies, grain interfaces) as shown in [12]. The first and second types of traps are usually manifested in hysteresis in the transfer and output characteristics, respectively.

As can be seen from the dependences shown in Figure 1, *a*, dark current is $\sim 10^{-10}$A when negative voltage is applied to the gate ($V_{GS} = -10$ V) due to semiconductor channel depletion, thus providing high signal-to noise ratio in the photo-FET mode.

For quantitative evaluation of hysteresis on the output characteristics, intrinsic resistance ratio of the channel in high-resistive and low-resistive states HRS/LRS is used:

$$HRS/LRS = R_{HRS} - R_{LRS},$$

where LRS is the low-resistance state (motion in direction (1) in Figure 1, *b*), and HRS is the high-resistance state (motion in direction (2) in Figure 1, *b*). The I-V curves show that the studied memtransistors have just a minor hysteresis of the transfer characteristic, and and hysteresis is most pronounced in the output characteristics. Hence, a conclusion may be made that defects in MoS_2, for example, at grain boundaries predominantly affect hysteresis in the studied devices. The set of photo-FET output curves shown in Figure 1, *b* demonstrates an increase in hysteresis as the voltage applied to the gate increases. The maximum HRS/LRS is 1.3 for device 1 and 1.6 for device 2.

Raman and PL spectra of the photo-FET channel at different V_{GS} are shown in Figure 2, *a, b*. Typical signs of an increase in electron concentration are the shift of the A_{1g} line in the Raman spectra towards low frequencies and broadening of this line, as well as a decrease in PL intensity simultaneously with the shift of PL maximum towards low energies due to a decrease in the intensity of a component corresponding to the neutral A exciton, and to an increase in the charged exciton (trion) component intensity. It is this effect that may be observed in the spectra of device 1 shown in Figure 2, *a, b*. The shift of line A_{1g} is $-0.7\,cm^{-1}$, and FWHM increases from 4.9 to 5.9 cm^{-1}. Such changes in the Raman spectra may be associated with an increase in electron concentration n_e from 2 to $4 \cdot 10^{12}\,cm^{-2}$ [13,14]. The shift of the PL maximum (Figure 2, *b*) is -30 meV. For

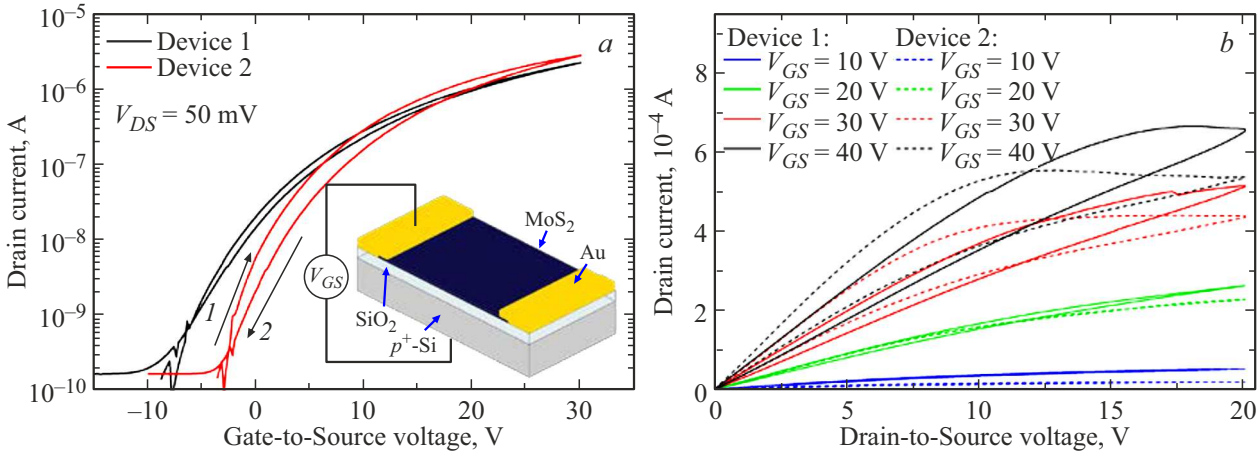

Figure 1. Transfer characteristics of the studied devices (*a*) and their output characteristics measured at different gate voltages (*b*). The inset shows a schematic drawing of the phototransistor structure of interest (photo-FET).

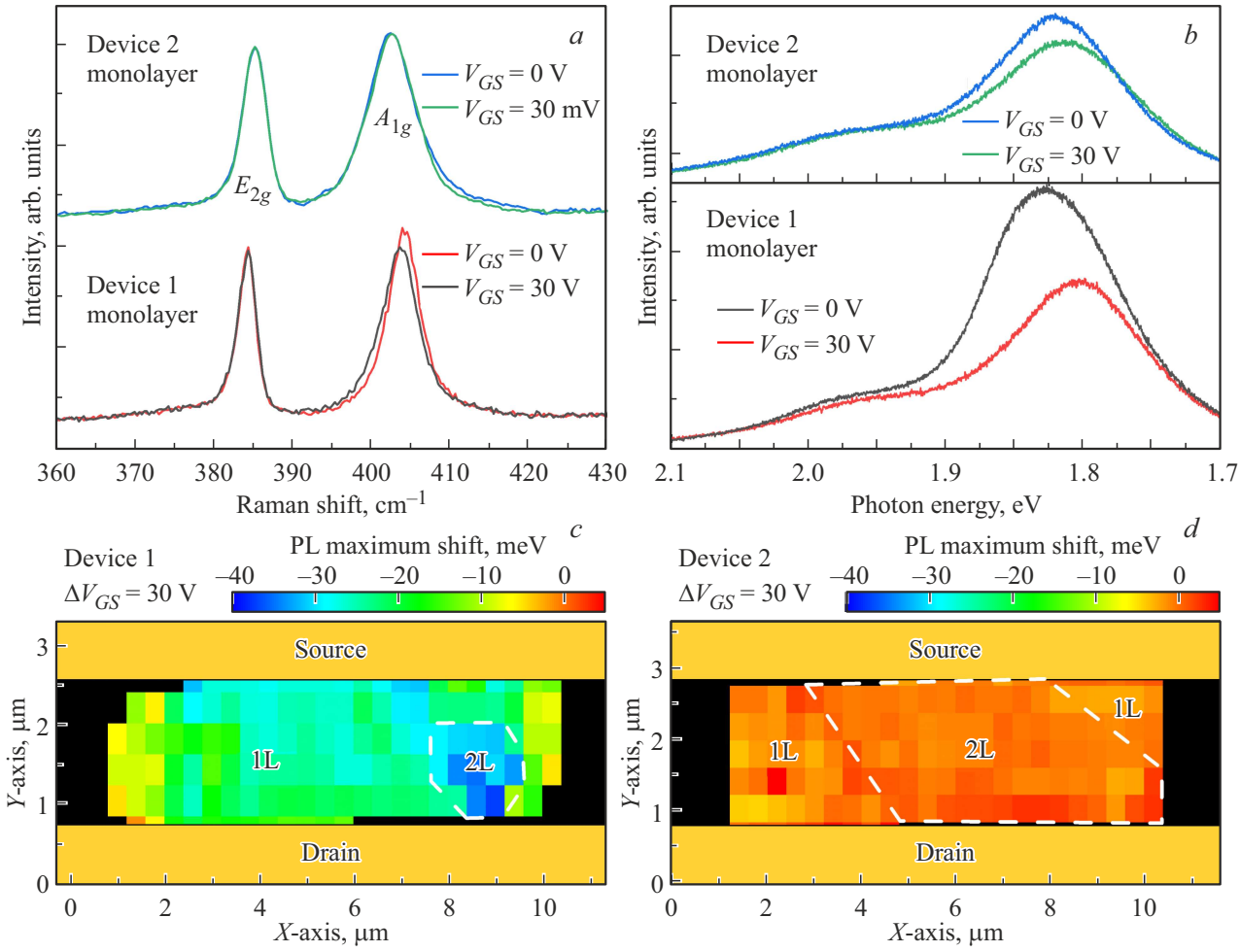

Figure 2. Typical Raman spectra (*a*) and PL spectra (*b*) measured in monolayer regions of the studied devices. Spectra of devices 1 and 2 are spaced vertically for convenience. *c, d* — maps of PL maximum shift in both devices. Source and drain contact positions are hereinafter shown schematically in yellow. Boundaries of two-layer (2L) regions are shown by a white dashed line.

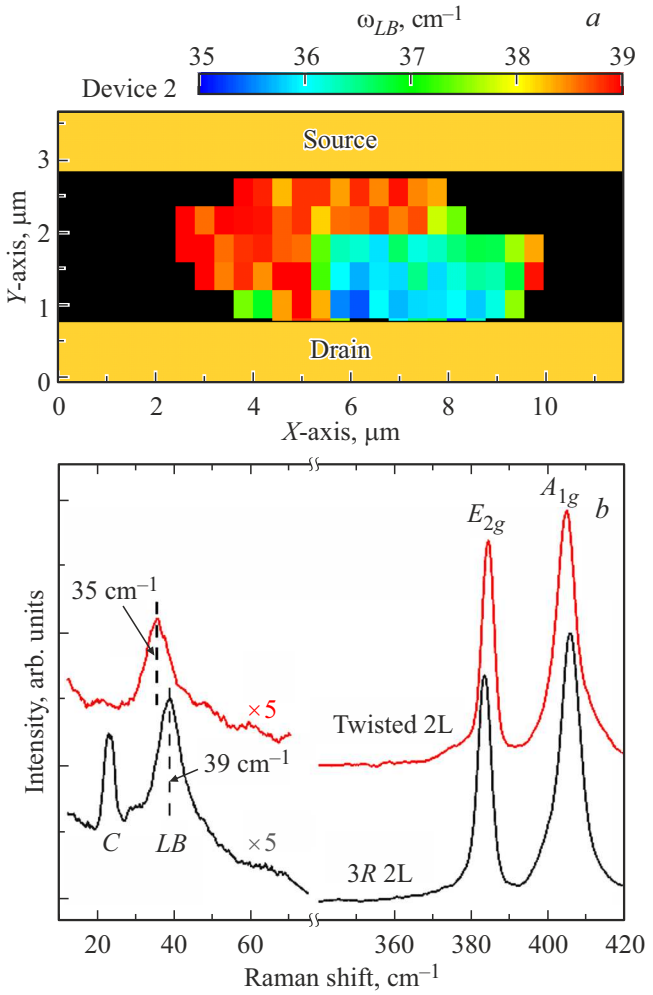

Figure 3. Raman map of the distribution of the „breathing" mode *LB* for device 2 (*a*) and the RS spectra typical for regions with $\omega_{LB} > 37\,\mathrm{cm}^{-1}$ and $\omega_{LB} < 37\,\mathrm{cm}^{-1}$ (*b*). For convenience, the spectra are spaced vertically, and the low-frequency component intensity is magnified fivefold.

device 2, the Raman spectra (Figure 2, *a*) are not subjected to significant changes as V_{GS} grows, however, the PL spectra (Figure 2, *b*) have a minor shift of the maximum (−5 meV), indicating a small ($\sim 1 \cdot 10^{12}\,\mathrm{cm}^{-2}$) increase in n_e.

Figure 2, *c* shows a map of the PL maximum in the structure with a small fraction of bilayer inclusions. Mean shift of the PL maximum in the monolayer regions is approximately −20 meV. The shift of the PL maximum in the bilayer regions is almost twice as large and is up to −40 meV. The same map for device 2 (Figure 2, *d*) demonstrates that there are almost no changes of the position of the PL maximum in the bilayer regions, however, a minor shift up to −5 meV is observed in the monolayer regions as shown above.

A weakly pronounced modulation of n_e by the gate voltage in device 2 with large fraction of two-layer inclusions is presumably associated with carrier recombination on defects, i. e. at grain boundaries and/or in twisted stacking regions. Figure 3, *a* shows the Raman map of the frequency distribution of the line of the „breathing" *LB* mode in the channel of device 2 and typical spectra for two regions: with higher and lower frequency ω_{LB}. While in the region with $\omega_{LB} > 37\,\mathrm{cm}^{-1}$, spectra correspond to bilayer 3*R*-MoS_2 [15], in region 2, the shear *C* mode line is absent, and the *LB* mode line is shifted towards low frequencies. According to the data in [16], this may be indicative of twisted MoS_2 layer stacking in the two-layer region. Twisted stacking, as mentioned above, may be induced by the build-up of an edge of one of the islands over the other edge. Note that device 2 demonstrated the highest hysteresis. Therefore, a conclusion may be made that multilayer regions or twisted packaging regions, besides grain boundaries, also play a role of hysteresis-inducing charge traps.

Summing up the aforesaid: Sensitivity of the CVD-MoS_2 channel of photo-FET structures to the applied gate–source voltage was studied in this work. It was demonstrated that the carrier concentration was more sensitive to gate voltage variation for the MoS_2 structures with small bilayer inclusions. As the fraction of bilayer inclusions with twisted stacking increases, the carrier concentration modulation by the gate decreases. It is suggested that this is caused by nonradiative carrier recombination on charge traps. Presence of carrier traps is connected to the occurrence of hysteresis on the output characteristics, which is necessary for creating memristor devices, however, it also causes a decrease in photosensitivity due to signal-to-noise ratio reduction in MoS_2-based photo-FETs. The data obtained in this work may potentially facilitate the development of procedures for selecting transistor structures based on polycrystalline CVD-MoS_2 with desired properties for future use in neuromorphic circuits assembled on a single chip. The question concerning the nature of charge traps an their connection with grain boundaries, twisted stacking regions or other factors is the topic for future research.

Conflict of interest

The authors declare no conflict of interest.

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