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Analytical models of depletion-layer capacitance of $p-n$ junction in high-voltage of mesaepitaxial semiconductors structures

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The article describes the results of researching and calculation of total depletion-layer capacitance of high-voltage, mesaepitaxial diodes. It is shown how influences of peripheral of mesa region for magnitude of total depletion-layer capacitance of $p-n$ junction in mesaepitaxial diodes structures it. Proposed of the analytical model of total depletion-layer capacitance of high-voltage, mesaepitaxial diodes structures, taking into account of the capacitance of peripheral of mesa region. The relations obtained of self-consistent of the analytical equations for the depletion-layer capacitance of mesa region for two options: for inclination angle constant of mesa chamfer; for variable angle inclination of mesa chamfer.

Keywords: mesa-epitaxial diode, mesa-region, mesa-chamfer, depletion-layer capacitance, capacitance–voltage characteristic.

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The development of techniques for the formation of a mesa-structured boundary in semiconductor multilayer epitaxial structures with $p-n$ junctions enables the fabrication of fast diode and transistor structures with operating voltages exceeding 1200 V. Multilayer mesa-epitaxial diode structures based on GaAs provide operating voltages higher than 2000 V. The system of electrical parameters and characteristics of the specified semiconductor devices features such a parameter as the $p-n$ junction capacitance at a fixed reverse bias [1]. The monitoring of electrical parameters of high-voltage mesa-epitaxial diode structures in the process of their production reveals a noticeable discrepancy between the calculated total depletion-layer capacitance of $p-n$ junctions and the data obtained experimentally. This discrepancy is innately attributable to the presence of a wide mesa region, which is a chamfer formed with a certain finite inclination angle. The authors of [2] have examined the influence of a positive chamfer with different inclination angles on the width of the space charge region (SCR) in structures with a p^+-n junction. However, no studies into the dependence of the depletion-layer capacitance on the chamfer size and its inclination angle in high-voltage mesa-epitaxial diode structures with both positive and negative chamfers have been published yet. Probing this issue, we obtained a unique result that is presented below.

The emergence of the so-called „residual“ (ΔC_{tot}), which is potentially commensurate with the design capacitance of a diode structure, may be determined quantitatively either by the difference between the calculated and experimental values of the total depletion-layer capacitance of a diode at the maximum reverse voltage or through the use of the „capacitance overlap factor.“ „Residual“ ΔC_{tot} tends to zero with an increase in area of a $p-n$ junction and increases as this area shrinks.

Figure 1, a presents the simplified physical structure of a high-voltage mesa-epitaxial diode under reverse bias, illustrating the distribution of space charge both in the bulk and in the mesa region (without account for distortions of the SCR boundaries on the surface of the mesa region) with the SCR spread into the anode p^+ region neglected.

Thus, with the SCR distribution in the peripheral mesa region taken into account, the total depletion-layer capacitance of high-voltage mesa-epitaxial diodes consists of two components: the design (active) one, which is specified by the design dimensions of the diode crystal with side a (the diode crystal reduced to a square), and the peripheral one, which is associated with the mesa region with a width of c (Fig. 1, a).

In view of this, the equivalent circuit of a high-voltage mesa-epitaxial diode should include an additional element: depletion-layer capacitance of the $p-n$ junction in the mesa region C_{jM} (Fig. 1, b).

Let us formulate a number of conditions for synthesis of a model of the total depletion-layer capacitance of a high-voltage mesa-epitaxial diode with analytical addition of the mesa region capacitance: the $p-n$ junction is sharp and asymmetric with a uniformly doped base; the $p-n$ junction is reverse-biased, making the SCR depletion approximation and the formula for capacitance of a planar capacitor applicable; the diode features a peripheral mesa region with a constant mesa chamfer inclination angle $\beta < 90°$; and the SCR width is the same in the design part of the diode crystal and the mesa region.

The data presented in Fig. 1, a are used to solve the problem at hand. We project the vertical structure onto

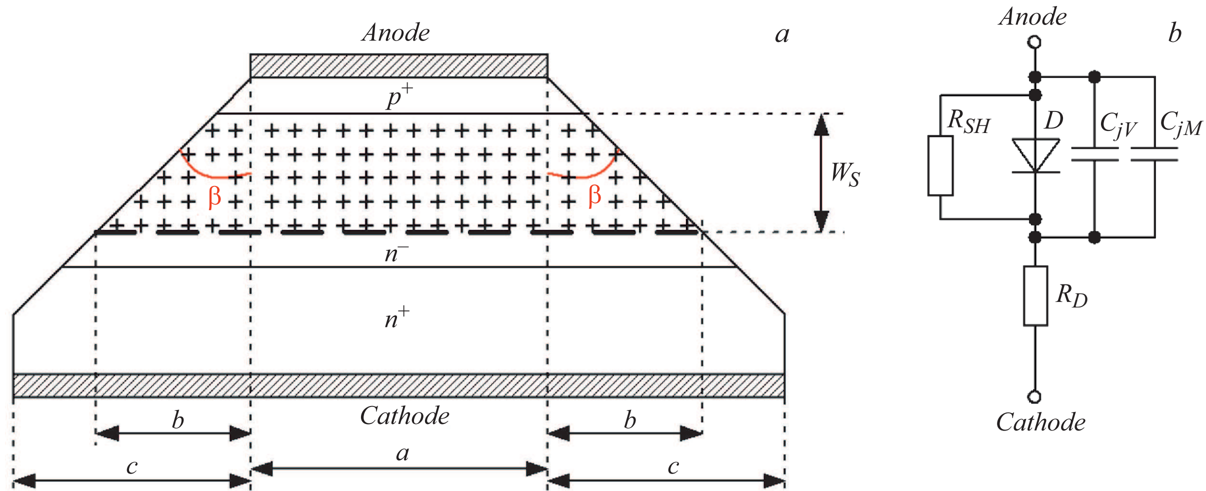

Figure 1. *a* — Physical structure of the high-voltage mesa-epitaxial diode crystal: β — mesa region inclination angle, a — side of the square anode region of the diode, b — length of the lower SCR boundary in the mesa region, c — mesa region width, and W_S — SCR width; *b* — equivalent circuit of the diode: D — ideal diode structure, C_{jV} — depletion-layer capacitance of the design part of the diode crystal, C_{jM} — depletion-layer capacitance of the mesa region of the diode crystal, R_D — series resistance of the diode formed by the ohmic resistance of the semiconductor material and the anode and cathode contacts, and R_{SH} — parasitic resistance shunting the $p-n$ junction.

a plane and apply the formula for capacitance of a planar capacitor to calculate the total depletion-layer capacitance of a high-voltage mesa-epitaxial diode [3]. The relation for depletion-layer capacitance of a $p-n$ junction is used in its differential form:

$$dC_{tot} = \frac{\varepsilon\varepsilon_0 dS(W_S)}{W_{S0}}, \tag{1}$$

where ε is the relative permittivity of the semiconductor material, ε_0 is the permittivity of vacuum, $S(W_S)$ is the $p-n$ junction area as a function of the SCR width, W_S is the SCR width, W_{S0} is the SCR width at zero external reverse bias voltage applied to the diode, and $dS(W_S)$ is the infinitesimal change in $p-n$ junction area at an infinitesimal change in bias voltage.

The projection of the physical structure of the diode crystal onto a plane allows one to present its area (the $p-n$ junction area) in the following form:

$$S(W_S) = a^2 + 4ab + 4b^2 = (a + 2b)^2$$
$$= (a + 2W_S \operatorname{tg}\beta)^2. \tag{2}$$

Variable quantity b (parameter) in relation (2) is written as $b = W_S \operatorname{tg}\beta$; i.e., variable b is the SCR width in the mesa region. The SCR width in the depletion approximation is characterized by the well-known relation [1,3].

Inserting the total differential of relation (2) into relation (1), we find the following:

$$dC_{jM} = \frac{4a\varepsilon\varepsilon_0 \operatorname{tg}\beta}{W_{S0}} dW_S + \frac{2\varepsilon\varepsilon_0 W_S \operatorname{tg}^2\beta}{W_{S0}} dW_S. \tag{3}$$

Integrating Eq. (3), we obtain a relation for capacitance of the mesa region of the high-voltage mesa-epitaxial diode crystal:

$$C_{jM} = \varepsilon\varepsilon_0 \operatorname{tg}\beta \frac{W_S - W_{S0}}{W_{S0}} [4a + (W_S + W_{S0}) \operatorname{tg}\beta]. \tag{4}$$

Actual high-voltage mesa-epitaxial diode structures have $-4a \gg (W_S + W_{S0}) \operatorname{tg}\beta$; therefore, relation (4) degenerates into a simple formula for depletion-layer capacitance of the mesa region:

$$C_{jM} = 4a\varepsilon\varepsilon_0 \operatorname{tg}\beta \frac{W_S - W_{S0}}{W_{S0}}$$
$$= P\varepsilon\varepsilon_0 \operatorname{tg}\beta \frac{W_S - W_{S0}}{W_{S0}}, \tag{5}$$

where $P = 4a$ is the perimeter of the mesa region of the diode crystal corresponding to the side lengths of its design part.

The relation for total depletion-layer capacitance of the $p-n$ junction of the high-voltage mesa-epitaxial diode crystal is as follows:

$$C_{tot} = C_{jV} + C_{jM} = \varepsilon\varepsilon_0 \frac{S_0}{W_S} + P\varepsilon\varepsilon_0 \operatorname{tg}\beta \frac{W_S - W_{S0}}{W_{S0}}, \tag{6}$$

where $C_{jV} = \varepsilon\varepsilon_0 S_0 / W_S$ is the design component of the total depletion-layer capacitance of the diode crystal specified by the photolithographic size of its active region (area S_0) and $C_{jM} = P\varepsilon\varepsilon_0 \operatorname{tg}\beta (W_S - W_{S0})/W_{S0}$ is the peripheral component of the total depletion-layer capacitance of the diode specified by the size and inclination angle of the mesa region chamfer.

The applicability of the depletion-layer capacitance model in the form of relation (6) is limited by the fact that

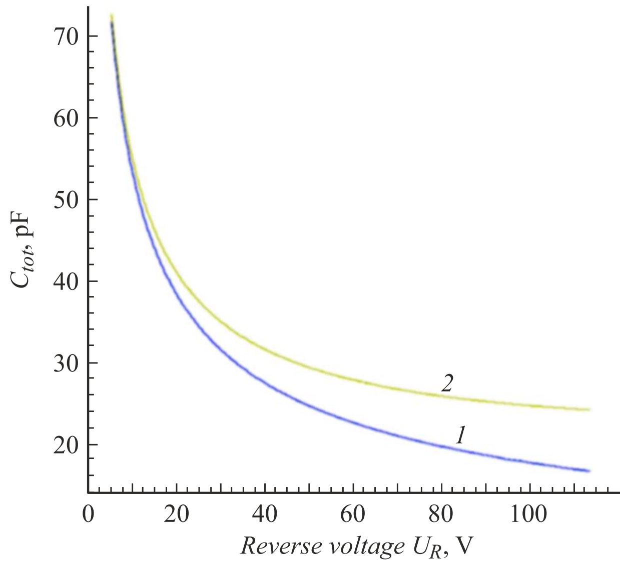

Figure 2. Capacitance–voltage characteristic of the depletion-layer capacitance of the p–n junction of the high-voltage mesa-epitaxial GaAs diode ($S_0 = 1.2 \cdot 10^{-2}\,\text{cm}^2$, $N_D = 2 \cdot 10^{15}\,\text{cm}^{-3}$, $T = 300\,\text{K}$) without the mesa chamfer influence (*1*) and with this influence taken into account ($\beta = 60^\circ$) (*2*).

inclination angle β of the mesa region chamfer is assumed to be constant in it. In view of this, relation (6) is applicable to those structures of high-voltage mesa-epitaxial diodes in which the shape of the mesa region allows for linear approximation with the determination of average inclination angle of the mesa region chamfer $\langle\beta\rangle$.

To extend the model of the total depletion-layer capacitance of a high-voltage mesa-epitaxial diode to mesa regions of arbitrary shape, we alter the requirement of constancy of the inclination angle of the mesa region chamfer, which may now be variable, in the list of initial assumptions. Thus, the total capacitance of the high-voltage mesa-epitaxial diode is a function of two variables (SCR width W_S and inclination angle of the mesa region chamfer β):

$$C_{tot} = f(W_S, \beta). \tag{7}$$

Let us consider an infinitesimal change in total capacitance of the varactor diode caused by an infinitesimal change in SCR width and inclination angle of the mesa region chamfer. Assuming linear independence of variables W_S and β, we suppose that there exists a non-zero second-order derivative

$$\frac{\partial^2 C_{tot}}{\partial\beta\partial W_S} = F(\beta, W_S) \neq 0. \tag{8}$$

Angle β is regarded as a parameter varying from 0 to $\beta < 90^\circ$. Let us write down relation (5) for an infinitesimal change in inclination angle β of the mesa region chamfer with a fixed SCR boundary W_S:

$$dC_{jM} = \left(P\varepsilon\varepsilon_0 \operatorname{tg}\beta \frac{W_S - W_{S0}}{W_{S0}}\right) d\beta. \tag{9}$$

Integrating relation (9) over parameter β, we obtain

$$C_{jM} = P\varepsilon\varepsilon_0 \frac{W_S - W_{S0}}{W_{S0}} \ln\left|\frac{1}{\cos\beta}\right|. \tag{10}$$

The total depletion-layer capacitance of the p–n junction of the high-voltage mesa-epitaxial diode with an arbitrary mesa region shape is

$$C_{tot} = C_{jV} + C_{jM} = \varepsilon\varepsilon_0 \frac{S_0}{W_S} + P\varepsilon\varepsilon_0 \frac{W_S - W_{S0}}{W_{S0}} \ln\left|\frac{1}{\cos\beta}\right|, \tag{11}$$

where $\beta < 90^\circ$ is the variable inclination angle of the mesa region chamfer.

Model (6) was used to calculate the depletion-layer capacitance of the p–n junction in the mesa region of the GaAs diode structure [3]. Figure 2 shows two calculated capacitance–voltage characteristics (CVCs) of the high-voltage mesa-epitaxial GaAs diode: CVC *1* was obtained without account for the mesa chamfer, while CVC *2* incorporates the influence of the mesa chamfer with inclination angle 60°. These calculated characteristics correspond to the experimental characteristics of high-voltage mesa-epitaxial GaAs diodes with their mesa regions formed by wet etching [4,5]. Figure 3 shows the CVCs of two identical high-voltage mesa-epitaxial GaAs diodes with different mesa region shapes.

Thus, analytical mathematical models of the total depletion-layer capacitance of high-voltage mesa-epitaxial

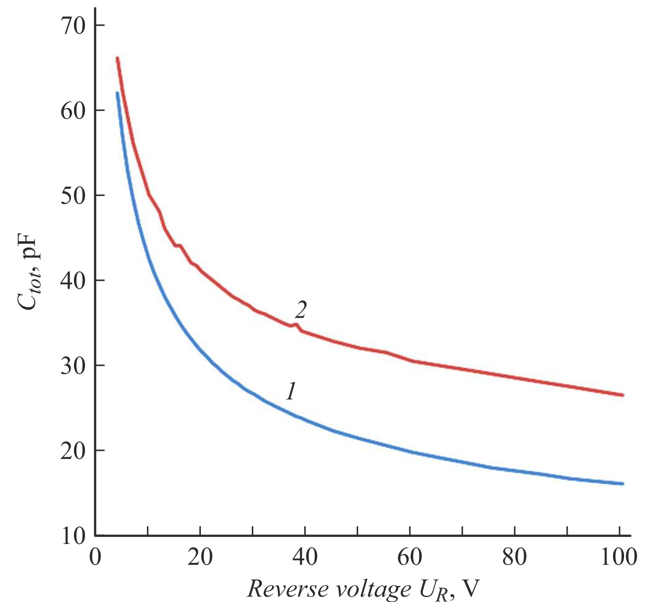

Figure 3. Experimental capacitance–voltage characteristics of the depletion-layer capacitance of p–n junctions of two high-voltage mesa-epitaxial GaAs diodes ($S_0 = 1.2 \cdot 10^{-2}\,\text{cm}^2$, $N_D = 2 \cdot 10^{15}\,\text{cm}^{-3}$, $T = 300\,\text{K}$). *1* — Diode with a mesa region obtained in a single cycle of selective wet etching ($\beta < 15^\circ$); *2* — diode with a mesa region obtained in two cycles of wet etching ($\beta \approx 60^\circ$).

structures with account for the contribution of the mesa region capacitance to the total depletion-layer capacitance of $p-n$ junctions were obtained. The models allow one to calculate with acceptable accuracy the capacitance–voltage characteristics of fast high-voltage mesa-epitaxial diodes, transistors, and high-voltage varicaps with arbitrary geometric shape of the mesa region within the entire operating range of bias voltages [6]. In addition, the obtained models provide an opportunity to perform non-destructive evaluation of the mesa region shape and calculation of the surface charge density in the mesa region.

Conflict of interest

The authors declare that they have no conflict of interest.

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