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Heterostructure with additional digital potential barriers for lownoise fieldeffect transistors

© S.A. Bogdanov, S.N. Karpov, R.A. Kotekin, A.B. Pashkovsky

JSC „RPC „Istok“ named after Shokin“, Fryazino, Moscow oblast, Russia
E-mail: solidstate10@mail.ru

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The paper presents the first results of a theoretical study of heterostructures for lownoise transistors with donoracceptor doping and systems of alternating thin AlAs/GaAs layers forming additional digital potential barriers. Introduction of digital barriers results in almost complete elimination of the channel of parallel conduction through a widebandgap material and significantly increases the drift velocity overshoot of electrons entering the highfield region, thus bringing the drift velocity overshoot in the relevant heterostructures closer to its theoretical limit implied in the model used, namely the overshoot of electron drift velocity in the undoped bulk material of the channel.

Keywords: digital potential barriers, fieldeffect transistor, electronsd́rift velocity overshoot.

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Since the first publications [1,2] till the present day, there have been carried out studies aimed at investigating and improving heterostructures for lownoise transistors (high electron mobility transistors, HEMT) [3–6]. Despite a significant progress in this field [7], such an important problem as parasitic conduction through a wide-bandgap material with direct electron scattering from dopants has not still been adequately solved for gallium-arsenide-based heterostructures, and remains important. As was shown for the first time more than 30 years ago [8,9], the transfer of hot carriers in the real space significantly affects the fieldeffect transistor noise ratio; this is also confirmed by recent studies [10,11]. At the same time, the problem of parasitic conduction in high-power transistors has already received several fairly efficient solutions, which have promoted a significant increase in the gain of produced devices [12] and development of heterostructure designs ensuring, as shown by the results of electron transport simulation, bringing the electron drift velocity overshoot to its theoretical limit [13,14]. What is interesting is to test the possibility of applying those engineering solutions also to heterostructures for lownoise transistors.

Fig. 1 demonstrates the band diagram of one of many options of a typical single-side-doped heterostructure $Al_{0.25}Ga_{0.75}As/In_{0.2}Ga_{0.8}As/GaAs$ for a lownoise transistor (HEMT). The calculation was performed based on solving a set of self-consistent Schrödinger and Poisson equations [15] with the boundary conditions conventional for problems of this kind (e. g. [16]). Thickness of the $Al_{0.25}Ga_{0.75}As$ layer between the surface and channel is 13 nm, width of the channel quantum well ($In_{0.2}Ga_{0.8}As$) is 12 nm; this layer is followed by an undoped GaAs layer 30 nm thick and a thick $Al_{0.25}Ga_{0.75}As$ layer. The first version of calculations assumed the absence of gate and the presence on the free surface of acceptor-type ionized surface states with surface density of $10^{12}\,cm^{-2}$. At the distance of 9.5 nm from the surface, the structure was δ-doped with the surface donor density $n_s = 4 \cdot 10^{12}\,cm^{-2}$. At the edges of the δ layer there were thin GaAs layers three monolayers thick. To facilitate the analysis, the dopant ionization was assumed to be 100%, i. e. the total surface electron density was $n_s = 3 \cdot 10^{12}\,cm^{-2}$ (including traps).

As previously noted more than once [7], it is clear that, in the case of such a high surface electron density, a significant part of charge carriers (in this case, about 25%) is located in the doped region of the wide-bandgap material even at room temperature, which gives rise to a channel of parallel conduction through the wide-bandgap material with direct scattering from ionized dopants. At the electron gas temperature of 1500 K, the electron fraction in the layer between the channel and surface increases to 30%. At first glance, it seems not very important for a lownoise transistor operating at the gate voltages close to the bias voltage; however, this effect degrades the device performance by inducing an increase in the source ohmic resistance and negatively affecting the dynamics of electrons entering and leaving the space under the gate and moving towards the drain.

As for the AlGaAs/GaAs structures, there are at least three extremely efficient ways to solve the problem of parasitic conduction: donor-acceptor doping [15], introducing digital barriers [14], and a combination of these methods.

Fig. 2 presents the band diagram of a Q-HEMT heterostructure differing from the initial HEMT structure in the presence of additional digital barriers and acceptor doping on the substrate side. The proposed improved version of the design of lownoise transistor heterostructure (Q-HEMT) implies that four AlAs digital barriers three monolayers thick each are inserted between the surface and δ layer. Two similar barriers are inserted into the spacer between

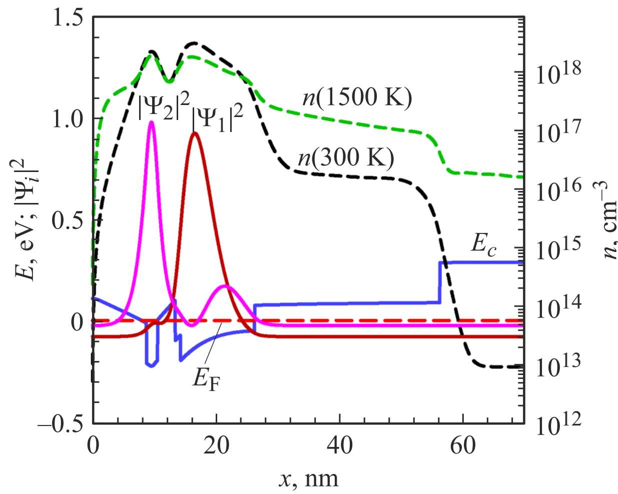

Figure 1. Band diagram of the lownoise transistor HEMT heterostructure; electron density and wave functions. Squared wave functions are plotted from respective levels.

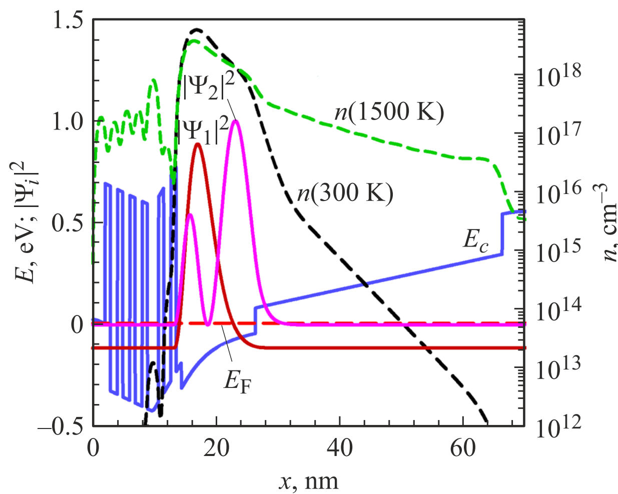

Figure 2. Band diagram of a heterostructure with additional digital barriers and acceptor doping on the substrate side; electron density and wave functions. Squared wave functions are plotted from respective levels.

the channel and δ layer. The GaAs layer is made 10 nm thicker, while the $Al_{0.25}Ga_{0.75}As$ layer edge on the substrate side is doped with an acceptor with the surface density of $0.5 \cdot 10^{12}\,cm^{-2}$ (acceptor doping was used to improve the transistor bias). The donor surface density in the δ-layer is increased by the same value. Thus, the electron surface density in the channel remained $n_s = 3 \cdot 10^{12}\,cm^{-2}$.

One can see that localization of electrons in such a structure is much stronger. For instance, at the electron gas temperature $T = 300\,K$, less than 0.03% of electrons are in the wide-bandgap material, while at $T = 1500\,K$ there are less than 3% of electrons. Due to this (Fig. 3), the electron drift velocity overshoot calculated for such a structure according to the model presented in [15] becomes close to that in the pure bulk material of the channel which is a theoretical limit for this model. Notice also that, in the structure with digital barriers, the distance between the first three quantum levels is significantly greater than the optical phonon energy; this can further increase the electron drift velocity in such structures [17]. Moreover, the ohmic contact of the fieldeffect transistor source consists of two parts: resistance of the contact itself, and resistance of the semiconductor region between the metal contact and gate. The latter will be undoubtedly lower in the Q-HEMT-based transistors, which is also expected to decrease the noise ratio.

The initial free-surface structure corresponding to the mode of a fully open transistor exhibits an almost twice lower drift velocity overshoot (HEMT, $U_g = 0$). At the gate voltages close to the bias voltage (when the potential changes relative to the free surface by the value $U_g = -0.75\,V$ $n_s \approx 2 \cdot 10^{11}\,cm^{-2}$), the drift velocity overshoot in such a structure also appears to be quite large (only 10% less than in the Q-HEMT structure). However, as noticed above, potential relief of the structure will change from completely open (when entering the space under the gate) to almost completely closed (at the drain edge) even under a very short gate; this will result in a decrease in the average drift velocity under the gate, and, hence, in an increase in the noise ratio.

In the proposed Q-HEMT heterostructure, the electron drift velocity overshoot is close to the theoretical limit for the model in question, that is, the electron drift velocity overshoot in the undoped bulk material of the channel. Hence, the best characteristics will be exhibited by the transistor based on the Q-HEMT structure [18]. Notice that a similar result was obtained for inverted structures

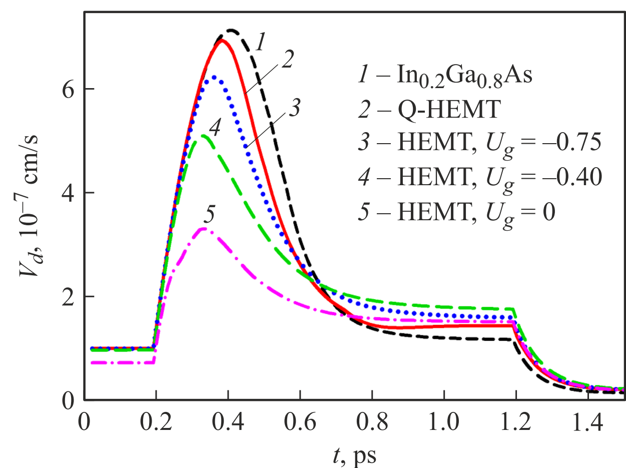

Figure 3. Drift velocity versus time for the electrons entering the highfield region. At $t < 0.2\,ps$ $E = 1\,kV/cm$; at $0.2 < t < 1.2\,ps$ $E = 20\,kV/cm$; at $t > 1.2\,ps$ $E = 1\,kV/cm$. Q-HEMT is the structure with digital barriers, HEMT is the initial structure with different gate voltages, $In_{0.2}Ga_{0.8}As$ is the bulk material of the channel. $U_g = 0$ corresponds to the structure option with the free surface in the absence of gate.

with digital potential barriers in [19] at the close values of the surface electron density in the channel. Therefore, in the course of assessing the practical feasibility of these structures, other factors may come out first, for example, manufacturability of the structures or transistors based on them.

Thus, in this study we have shown that introducing digital potential barriers into the heterostructures of low-noise fieldeffect transistors can eliminate from them the channel of parasitic conduction through the doped wide-bandgap material. The calculations have demonstrated that the electron drift velocity overshoot in such structures approaches its theoretical limit, namely the drift velocity overshoot in the channel bulk material. Therefore, in devices based on Q-HEMT-structures, the average electron velocity under the gate will increase, which will increase the device operating frequencies and reduce the noise ratio.

Conflict of interests

The authors declare that they have no conflict of interests.

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