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Spatial inhomogeneity of impact-ionization switching of power silicon thyristors

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Research has been carried out on the process of switching a power silicon thyristor with a voltage pulse. It has been established that when the voltage rise rate dU/dt increases from 1 to 10 kV/ns, the switching voltage increases from 3 to 7 kV, and the duration of the switching process is reduced to 200 ps. A thyristor with a pre-applied bias voltage has a shorter duration and a higher switching voltage compared to a thyristor without it. At $dU/dt > 4$ kV/ns, the switching voltage of the thyristor without bias becomes more than that of the thyristor with bias, which is associated with saturation of the carrier velocities in the neutral part of the n*n*-base. Simulation has shown that the calculated and experimental voltage oscillograms have quantitative agreement in the case when the value of the active area of the structure through which the switching current passes increases with increasing dU/dt, approaching the total area of the device at $dU/dt > 10$ kV/ns and tends to zero at $dU/dt < 1$ kV/ns. It is shown that spatial inhomogeneity of the current distribution arises at the stage of formation of the impact-ionization front in a region depleted of majority charge carriers. The size of the active area is proportional to the maximum intensity of ionization processes in this time interval.

Keywords: impact ionization in semiconductors, current inhomogeneity in semiconductors, picosecond switching of semiconductor devices.

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Introduction

Identification of the effect of subnanosecond switching of a semiconductor diode [1] under action of voltage pulse increasing with rate $dU/dt > 1$ kV/ns, resulted in creation of a class of powerful subnanosecond semiconductor switches [2–6]. Switching mechanism was discussed in large number of papers and is generally associated with quick resistance of semiconductor structure as result of ts filling with dense plasma after shock-ionization TRAPATT waves [3,7]. Speed of such waves movement exceeds the saturated speed of movement of carriers and is limited only by light speed in semiconductor.

Issue of heterogeneity of the switching process was raised before [8–12], and last time the interest to it significantly increased [13–20]. To characterize the degree of heterogeneity a value of active area S_a is introduced as part of the device area participating in switching process. It was determined that significant effect on value of Sa is made by voltage increasing rate dU/dt on semiconductor structure before its transition to conductive state. Active area was observed visually in form of glow when switching GaAs diodes [8,9]. In [8] we observed separate glow channels, their number increases with dU/dt increasing. In [9] at dU/dt of tens of kV/ns the homogeneous over entire area diode glow was observed.

In devices,where silicon or other indirect band gap semiconductors are used as material, the visual evaluation of the active area is impossible. Methods ensuring indirect evaluation, for example, comparison of calculation results obtained at different values of the active area, with experimental oscillograms. Selecting the calculation result which has minimum difference from the experimental result, we can evaluate the active area. This method in [19] provide evaluations of the active area involved in switching of powerful thyristors with pre-applied bias voltage under action of voltage pulse increasing with rate $dU/dt = 0.8-6$ kV/ns. The thyristors made of *n*-silicon with different resistivity (80 and 105 Ω·cm) and diameter 32 and 40 mm were used. In [20] the method was used when studying the switching of silicon diode 6 mm in diameter with resistivity 32 Ω·cm. The bias voltage was not pre-applied, and voltage increasing rate was in range $dU/dt = 1.5-10$ kV/ns. In all cases it was identified that calculations well describe the experimental results only at definite type of active area value dependence on dU/dt. Active area increases with increase in dU/dt, it monotonically approaches total area of device at $dU/dt > 10$ kV/ns. With dU/dt decreasing the active area value decreases, tending to zero at $dU/dt < 1$ kV/ns. This agrees with experimentally determined the disappearance of the fast switching effect in silicon thyristors at $dU/dt < 0.5$ kV/ns [17] and monitoring breakdown homogeneous over area of GaAs-diodes at dU/dt of tens kV/ns[9].

In practice the heterogeneity of current distribution over the device area affects its quick response, voltage drop on

it and losses of energy in device at stage of current flow. The recent studies found that increase in dU/dt from 0.5 to 6 kV/ns decreases the time of thyristor transition into conductive state to 200–300 ps [17–22], increases temperature of semiconductor structure, when the quick switching effect is implemented, to 180°C [21], and due to increase in active area the energy losses in the thyristor decrease by 1.5–3 times when the discharge current of a capacitive storage device passes through the thyristor [18,22].

Large interest is paid to operation modes when there is not pre-mixing on device. For example, semiconductor diode and thyristor front edge sharpeners embedded in the inner conductor break of a coaxial power transmission line operate in this mode [6,16,23]. When diodes and thyristors are connected in series, the switchable power reaches hundreds MW with front edge width of a few tens of picoseconds [24].

In present paper we studies experimentally and theoretically the process of thyristor switching by voltage pulse increasing with rate dU/dt below 10 kV/ns. Studies were performed both in mode with pre-applied bias voltage ($U_0 = 2.2$ kV), and without it. For more complete analysis of spatial heterogeneity effect on the switching process in silicon devices in paper we used data of study of switching the silicon diode without bias voltage at dU/dt in range 1–10 kV/ns [20].

1. Experiment

1.1. Experiment scheme.

In present paper the process of switching the thyristor from interlocking state to conductive state without further power current flow from external circuit. Scheme of experiment (Fig. 1) comprises a capacitor $C1 = 1.3\,\mu$F, charged to bias voltage $U_0 = 2.2$ kV of negative polarity. The bias voltage by switch S (thyristor or transistor) via a resistor $R1 = 86\,\Omega$ is supplied to studied thyristor T. Full time of bias voltage setting on the thyristor T is $\sim 10\,\mu$s. After time delay $50\,\mu$s a start pulse is applied to the thyristor from small-size solid-state generator which output unit is a coaxial 50-Ω oil-filled line (*1* in Fig. 1). Start pulse of negative polarity is applied via isolating capacitor $C2 = 4.7$ nF, installed inside the line *1*, and is registered by capacitive sensor *2*. The pulse amplitude at line output during its operation to the matched load is adjustable in the range from 50 to 100 kV, pulse front at level 0.1–0.9 of amplitude — ~ 1 ns, pulse width at half maximum — ~ 4 ns. Increasing rate of voltage acting on the thyristor dU/dt in range 5–10 kV/ns varies with amplitude regulation the start pulse, and change in value of dU/dt in range 0.5–5 kV/ns is achieved by installation of the additional resistor $R2$ with different resistance.

As thyristor T in the experiments the semiconductor element of industrial low-frequency thyristors was used having tablet form of grade T133-320-22. The thyristor has the following passport parameters: work DC voltage — 2.2 kV (voltage class — 22), shock current amplitude — 6 kA, critical increasing rate of current upon switching on via control electrode — 100 A/μs. The semiconductor element has diameter 32 mm and height 2 mm, of which anode cooling disk made of molybdenum occupies 1.4 mm. The thyristor semiconductor element has structure of p^+-p-n-p-n^+-type 520 μm thick, and manufactured according to diffusion technology of silicon of n-type with resistivity $\rho = 80$–$85\,\Omega\cdot$cm.

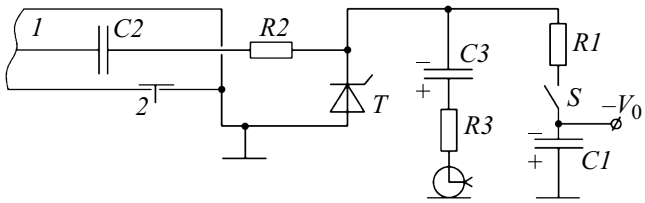

Figure 1. Scheme of the experimental setup.

Process of thyristor switching into conductive state was registered using resistive voltage divider with elements $C3$ and $R3$ (Fig. 1). The top arm of divider is resistor $R3$, and bottom arm is formed by registration cable with wave resistance 50 Ω. The capacitor $C3$ isolates the divider from constant bias voltage U_0. To reduce self-inductance of the divider elements the capacitor $C3$ is made of foiled mylar film 50 μm thick, and the resistor $R3$ is partially screened by the metering cable braiding. The voltage divider was connected directly to the contacts of semiconductor element. Own time of signal increasing at the divider output determined during calibration was ~ 180 ps at level 0.1–0.9 of amplitude. In the registration channel the signal attenuators was used with bandwidth 18 GHz, and as recorder the oscilloscope DPO 70404C with bandwidth 4 GHz was used. Final oscillogram was obtained by superposition and averaging of 10 consecutive pulses.

1.2. Experimental results

The experimentally obtained oscillograms of voltage on thyristor at various voltage increasing rates dU/dt are given in Fig. 2. Part of experimental results in Fig. 2, a at $dU/dt < 4$ kV/ns was taken from paper [21]. It is obvious that during switching of both thyristor with pre-applied bias voltage (Fig. 2, a), and without it (Fig. 2, b), with increase in dU/dt the amplitude of switching voltage increases, and switching time decreases.

Voltage oscillations on oscillograms in Fig. 2 after quick (subnanosecond) thyristor transition into conductive state, superimposed on level of residual voltage, are not associated with processes occurred inside the semiconductor structure. Oscillations are due to excitation of L–C-circuits formed by inductance of divider connection to the semiconductor element (~ 6 nH) and capacitance of capacitor plates $C3$ to earth (~ 10 pF).

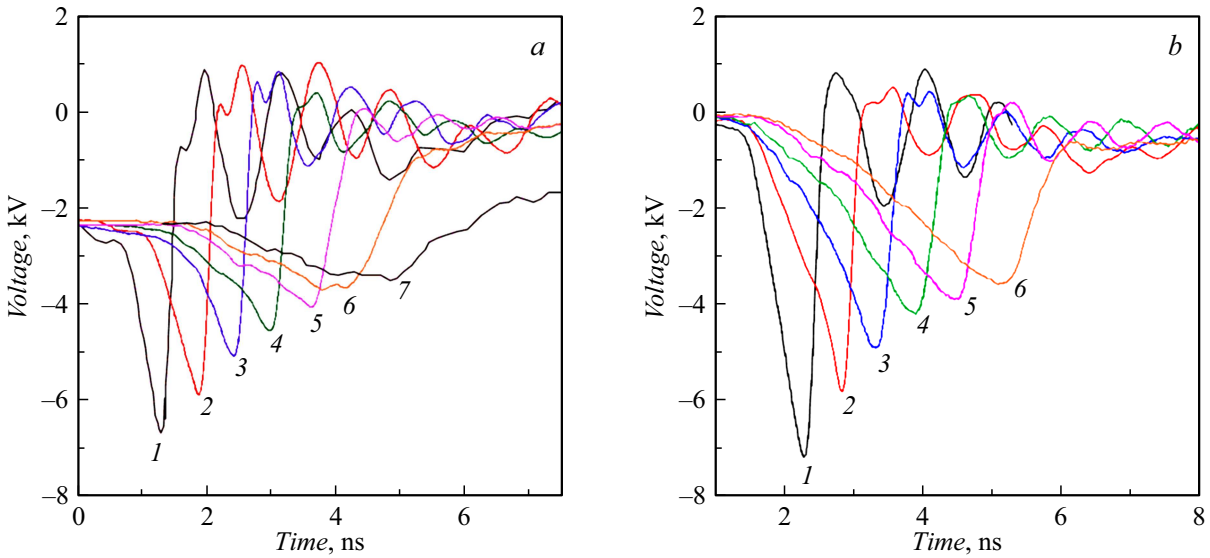

Figure 2. The experimental dependences of voltage on thyristor on time with bias voltage (*a*) and without it (*b*). Value dU/dt in kV/ns is: *a* — 7.5 (*1*), 4.7 (*2*), 3.3 (*3*), 1.6 (*4*), 0.9 (*5*), 0.7 (*6*), 0.7 (*7*); *b* — 9 (*1*), 4.3 (*2*), 2.9 (*3*), 2 (*4*), 1.6 (*5*), 1.3 (*6*). (Do=igits in brackets designate curve number in Figure.)

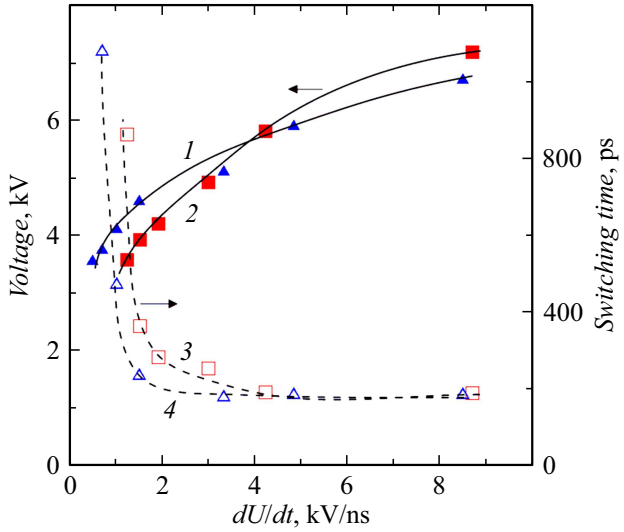

Figure 3. Maximum voltage (dark triangles and squares) and switching time (light triangles and squares) vs. increasing rate of voltage on thyristor with applied bias voltage (triangles) and without it (squares) respectively.

Fig. 3 shows results of processing the experimental oscillograms in form of dependences of switching voltage and switching time (by level 0.1−0.9 of voltage amplitude). We can note that increase in dU/dt from 1 to 10 kV/ns significantly changes switching characteristics of thyristor: switching voltage increases by two times, and time of its transition into conductive state decreases by 4−5 times reaching 200 ps. Voltage amplitude increasing corresponds to increase in electric field strength in the device structure, which results in increase in movement speed of shock-ionization waves and reduces the time of structure filling with plasma, and therefore the switching time.

From Fig. 3 we see that duration of the switching process increases upon decrease in dU/dt, and in the vicinity of $dU/dt \sim 1$ and 1.5 kV/ns asymptotically increases for thyristor with and without applied bias, respectively. These values correspond to minimum values of dU/dt, below which the effect of quick switching disappears. Existence of effect border was shown earlier [17].

At low values of dU/dt switching of the thyristor with bias voltage occurs quicker and at larger voltage amplitude then of the thyristor without bias. But at $dU/dt > 4$ kV/ns value of the switching voltage of thyristor without bias becomes larger then in thyristor with bias (Fig. 3). This is due to change in the geometry of the electric field distribution in the thyristor structure, which is discussed in more detail below in Sec. 2.2.

2. Calculation part

2.1. Model description

For calculations the model meaning the joint solutions of equations describing the operation of experiment electric circuit comprising semiconductor device, and equations describing the dynamics of electrons, holes, electric field and temperature in device structure. dynamics of electrons and holes the continuity equations are used, and the Poisson equation is used for the electric field. Calculations consider carrier velocity dependences on va;ues of electric field, temperature, scattering on impurities and electron-hole scattering. The processes of avalanche multiplication, tunneling carrier generation, and ionization of deep impurities were

taken into account [25]. Avalanche multiplication coefficients were taken in form [21] ensuring their dependence on the electric field and temperature. Calculation considered the dependence of intensity of ionization processes on concentration of carriers due to electron-hole scattering [25].

In calculations the actual distribution of impurities in the structure of the thyristor under study is taken into account (T133-320-22). The thyristor had structure of p^+-p-n-p-n^+-type 520 μm thick and were manufactured of the silicon of n-type with resistivity $\rho = 80\,\Omega\cdot$cm ($Nd \sim 0.6 \cdot 10^{14}\,\mathrm{cm}^{-3}$) and 32 mm in diameter. The doping impurities are distributed as follows: p^+-region was formed by diffusion of boron ($10^{18}\,\mathrm{cm}^{-3}$, 50 μm), p-regions — by diffusion of aluminium ($2 \cdot 10^{16}\,\mathrm{cm}^{-3}$, 85 μm), n^+-region — by diffusion of phosphorous ($10^{19}\,\mathrm{cm}^{-3}$, 20 μm).

For more complete analysis of current spatial heterogeneity effect on the switching process in present paper we used results of study of switching the silicon diode without applied bias voltage. The diode had structure of p^+-p-n-n^+-type 350 μm thick and with diameter 6 mm at resistivity n-silicon $\rho = 32\,\Omega\cdot$cm ($Nd \sim 1.5 \cdot 10^{14}\,\mathrm{cm}^{-3}$). Impurities are distributed in the diode structure as follows: p^+-region was formed by diffusion of boron ($10^{19}\,\mathrm{cm}^{-3}$, 80 μm), p-region — by diffusion of auminium ($10^{17}\,\mathrm{cm}^{-3}$, 136 μm), n^+-region — by diffusion of phosphorous ($10^{19}\,\mathrm{cm}^{-3}$, 60 μm) [20]. Digits in brackets are limit concentration and depth of location of impurities in device structure.

Operation of experimental electric circuit in calculation of diode switching is set by telegraph equations [21], of thyristor — by Kirchhoff's equations [19].

In [26] it was suggested to include multiplication processes after reaching the carrier concentration of n_0 to prevent the influence of avalanche propagation of unphysically small concentrations of carriers. Introduction of such condition is also associated with limitations of drift-diffusion approximation used in calculations. Such approach was widely used in [17,19,27,28].

Significant effect on the switching process in silicon structures can be provided by ionization of deep levels of M-type with energy 0.54 eV [28]. Concentration N_{PI} of such levels remains the study theme. In [29] it was shown that value of N_{PI} is in range $10^{11}-10^{13}\,\mathrm{cm}^{-3}$. But [30] showed that in structures of p^+-n-n^+-type these levels are absent, and in structures of p^+-p-n-n^+-type they present. In present paper we accepted $N_{PI} = 10^{12}\,\mathrm{cm}^{-3}$ and $n_0 = 0.5 \cdot 10^9\,\mathrm{cm}^{-3}$, which ensured good agreement of the calculation results and the experimental data in [17].

To consider the spatial heterogeneity the calculation accepted that in switching process not all device area was used. Part of area, through which the switching current flows, is called as active area S_a, and the rest part — passive area. Calculations further use parameter $K = S/S_a$, suggested in [10]. Assuming that current in parts is distributed homogeneously along the area, the one-dimensional equations of the dynamics of carriers and field in the active and passive parts of the device can be solved. It is Structure division into active and passive parts occurs when the field strength reaches the ionization threshold at any point of the structure:

$$E > E_b, \tag{1}$$

where $E_b = 1.8 \cdot 10^5$ V/cm — the electric field value corresponding to the ionization threshold in silicon. After division the ionization processes in model develop in active part only, and in passive part of the device the ionization process are absent. Note that changing the value of E_b in the range from 0 to $2 \cdot 10^5$ does not affect the calculation results.

2.2. Switching process

Let's compare the process of thyristor switching with and without bias voltage. For this we select calculation results in Fig. 6, *a* and *b* with close values of increasing rate of voltage pulse. Fig. 4, 5 show calculation results of switching process at $4dU/dt \sim 4$ kV/ns, corresponding to curves 2 in Fig. 6, *a* and *b* at $K = 4$ and $K = 3.5$. For convenience, the voltage, current, and electric field strength in the Figures are given in positive polarity. Fig. 4 shows switching stages of thyristor with applied bias voltage: stage of amplitude increasing of electric field and width of space charge region (SCR) until start of the shock-ionization front edge ($0-t_1$), stage of structure filling with plasma due to propagation of shock-ionization front edge in SCR and one-dimensional breakdown in neutral part of n-base (t_1-t_2), stage of switching to maximum current through the active part of the structure (t_2-t_3), and final switching stage ($t > t_3$). The same stages are identified also during switching the thyristor without bias voltage with appropriate ranges ($0-t_4$), (t_4-t_5), (t_5-t_6) and ($t > t_6$). In this case the voltage pulse is applied to structure filled with equilibrium charge carriers, ans at the first stage ($0-t_4$) initially in vicinity of n-p-transition SCR is formed. When switching the thyristor with bias voltage before the voltage pulse reception SCR already exists in the structure.

For further analysis we introduce the integral factor considering the intensity of ionization processes in semiconductor structure

$$IF = \int_0^W \alpha(E) \cdot dx, \tag{2}$$

where α — ionization coefficient, W — structure size. Value IF is numerically equal to the number of electron-hole pairs, occurred due to avalanche multiplication when single carrier passes through region of strong electrical field. Integral factor IF is a suitable indicator of processes occurring in device structure. Its value dependence on time is shown by curves *9* and *10* in Fig. 4. Maxima IF_1, IF_2, IF_3 are related to the process of formation of shock-ionization front edge in SCR, ionization processes in n-base and in

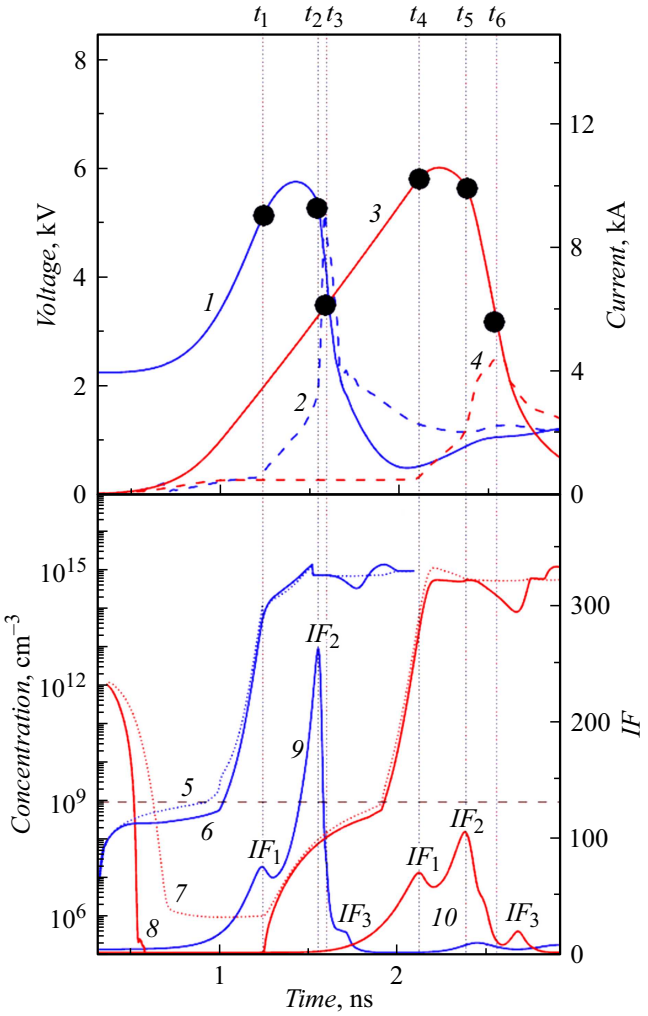

Figure 4. Calculation dependences of voltage (*1* and *3*), current through active part of structure (*2* and *4*, dashed curves), maximum concentration of holes (*5* and *7*, dot curved) and electrons (*6* and *8*) in SCR, integral factor (*9* and *10*) on time for thyristor with bias voltage and without it, respectively. The calculations were made at $K = 4$ for the thyristor with bias voltage and at $K = 3.5$ without it.

narrow regions beyond the filled with plasma of *n*-base respectively.

Let's consider process of switching in structure of thyristor with pre-applied bias voltage. In thyristor structure before supply of the voltage pulse there is region free of basic charge carriers (SCR), voltage in which is equal to bias voltage $U_0 = 2.2$ kV, and concentration of carriers does not exceed 10^6 cm^{-3}. At stage $(0-t_1)$ when the voltage pulse is applied, SCR width and field amplitude began increasing. The observed increase in concentration of holes and electrons (curves *5* and *6* in Fig. 4) is associated with processes of tunnel ionization of deep levels.

When concentration $n_0 \sim 10^9$ cm^{-3} is reached (shown by dashed line in Fig. 4) the processes of avalanche multiplication are activated, and further more quicker increase in carriers concentration is linked with this. At this stage the field amplitude reaches the ionization threshold, and the thyristor structure according to model condition (1) is divided into active and passive parts. Further calculations of dynamics of electrons, holes and field in parts are made independently provide that ionization processes in passive part are switched off. At time moment t_1 the integral factor achieves maximum IF_1 (curve *9* in Fig. 4), and concentration of electrons and holes becomes equal to level of base doping $N_d \sim 0.6 \cdot 10^{14}$ cm^{-3} (curves *4* and *5* in Fig. 4) and sufficient to compensate the field created by charge of fixed ions of donors and acceptors. Time required for this corresponds to Maxwell relaxation time:

$$t_M \sim \frac{\varepsilon \cdot \varepsilon_0}{n \cdot \mu_n \cdot e}, \qquad (2)$$

where n, μ_n, e — concentration mobility and charge of electrons; ε — electric constant; ε_0 — dielectric constant of silicon. Assuming $n = N_d$, we obtain evaluation of time $t_M \sim 100$ ps, which practically coincide with width of peak IF_1 at height of nearest minimum in curve of the integral factor (curve *9* in Fig. 4). Holes and electrons formed during ionization form the maximum of concentration in SCR (curves *1* in Fig. 5, *a*). Moving to opposite sides holes and electrons created charge which field compensates the external field thus resulting in field decreasing om place of maximum of concentration (curve *1* in Fig. 5, *a*). The restructuring of the field distribution leads to decrease in the intensity of ionization processes and the minimum formation on the integral factor curve. Region of string field shifts, further within it the process of intensive ionization start, and process repeats. SCR filling with plasma occurs with movement speed of strong field region, which mandatory exceeds the saturated speed of carriers $V_s = 10^7$ cm/s. This mechanism is close to known TRAPATT-waves in semiconductors [7]. Speed of movement of such waves is limited by light speed in semiconductor.

At stage (t_1-t_2) shock-ionization front edges move to both sides from plane of *n*-*p*-transition, filling SCR with dense electron-hole plasma. Movement speed of front edges up to five times exceed value of V_s. Simultaneously the ionization processes occur in each point of the neutral part of *n*-base (curves *2* in Fig. 5, *a*). Plasma density increasing results in the moment when the active part voltage of thyristor starts decreasing. At time moment t_2 plasma completely fills SCR (curves *2* in Fig. 5).

At stage (t_2-t_3) structure filling with plasma continues, mainly due to ionization processes in each point of *n*-base, located beyond SCR filled with plasma (curves *2,3* in Fig. 5, *a*). Structure resistance decreasing results in capacitor discharge of p[assive part and increase in current through active part of the thyristor (dashed curve *2* in Fig. 4) Amplitude of current density flowing through active part of the device ($K = 4$ or $\sim 25\%$ of total area) reaches 5 kA/cm^2. Current density increasing increases intensity of the ionization processes, which decreases time for filling with plasma of the active part and duration of device switching. If we

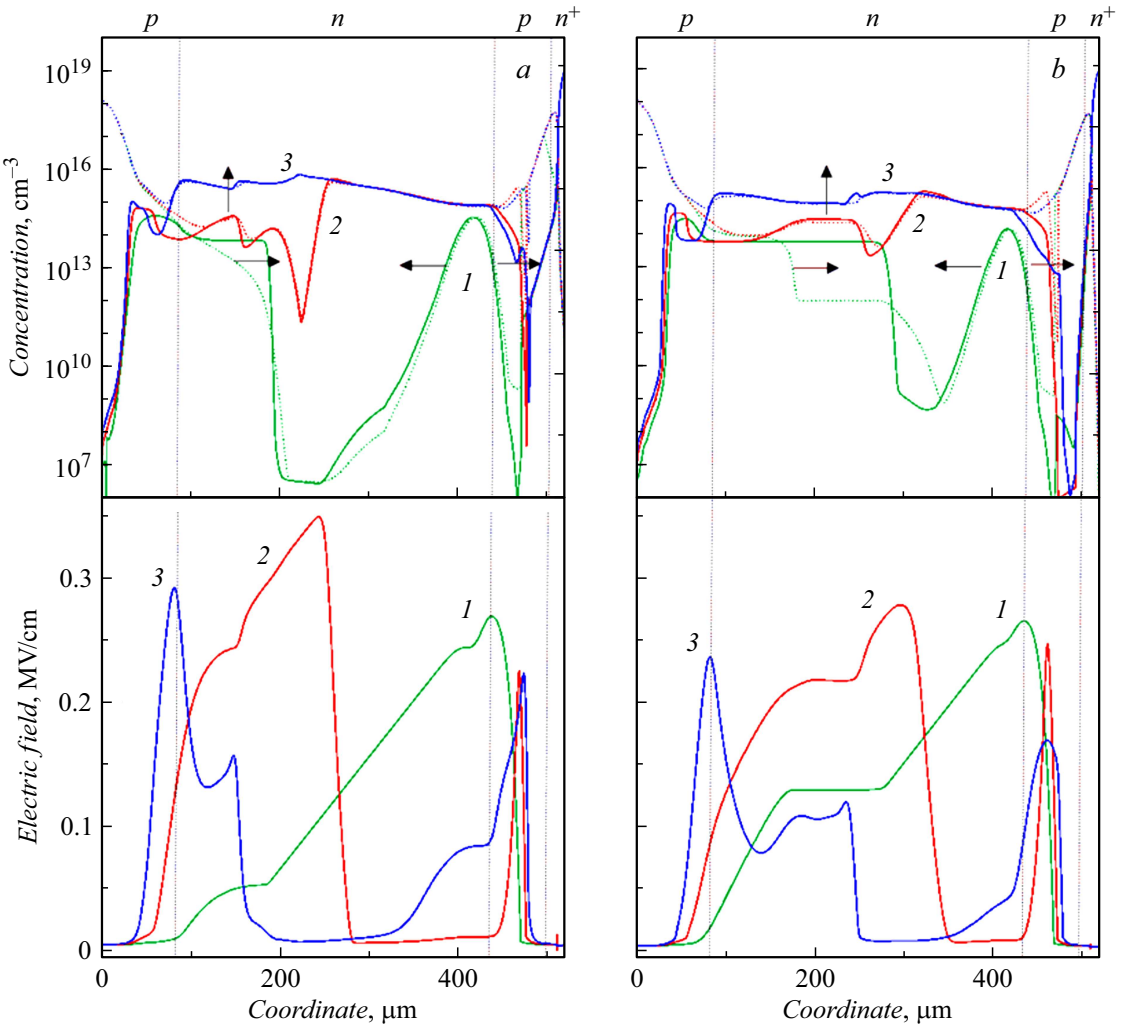

Figure 5. Distributions of concentrations of holes (dotted curves), electrons (solid curves) and electric field strength in active part of structure during switching the thyristor with applied bias voltage (*a*) and without it (*b*). *a* — *1–3* correspond to time moments t_1-t_3, *b* — time moments t_4-t_6 in Fig. 4. The arrows indicate the direction of motion of the ionization front edges.

do not consider the spatial heterogeneity of the switching process, then the density of the current flowing through the device at the switching stage will drop significantly, and the duration of the switching process will increase by several times and become more than nanosecond (dashed curve). *2* in Fig. 6, *b*).

In passive part of the device due to the ionization processes absence the dynamic of electrons, holes and field is simple and is not shown in Figures. With increase in voltage on device SCR width and field amplitude in passive part increase, and respectively decrease with voltage decreasing. Note that charge into passive part enters via the active part, where it occurs in ionization processes.

At moment t_3 *n*-base is filled with plasma with density $\sim 5 \cdot 10^{15}\,\mathrm{cm}^{-3}$. The field is displaced to narrow regions beyond the plasma (curves *3* in Fig. 5, *a*). Further, as a result of the ionization processes development, these regions of the field are also filled with dense plasma. At this stage the integral factor has maximum IF_3, its amplitude is small (curve *9* in Fig. 4) due to narrow regions of strong field.

So, we can distinguish three successive stages of structure filling with plasma: using shock-ionization waves, propagating in SCR, due to ionization processes in each point of *n*-base, located beyond SCR filled with plasma, and by wave method in narrow regions of the field located beyond the *n*-base filled with plasma. The shock-ionization waves propagation in SCR starts at stage of voltage pulse increasing, and ends at the beginning of stage of voltage decreasing. Major part of the switching process occurs as a result of device resistance decreasing at second and third stages of the structure filling with plasma. The discharge of the passive part of the structure causes a quick increase in current in the active part, which significantly accelerates the process of the structure filling with plasma and reduces the duration of the switching process.

Such scenario is similar to „two-key“ mechanism of switching the thyristor in [19], where initially *n*-base is filled

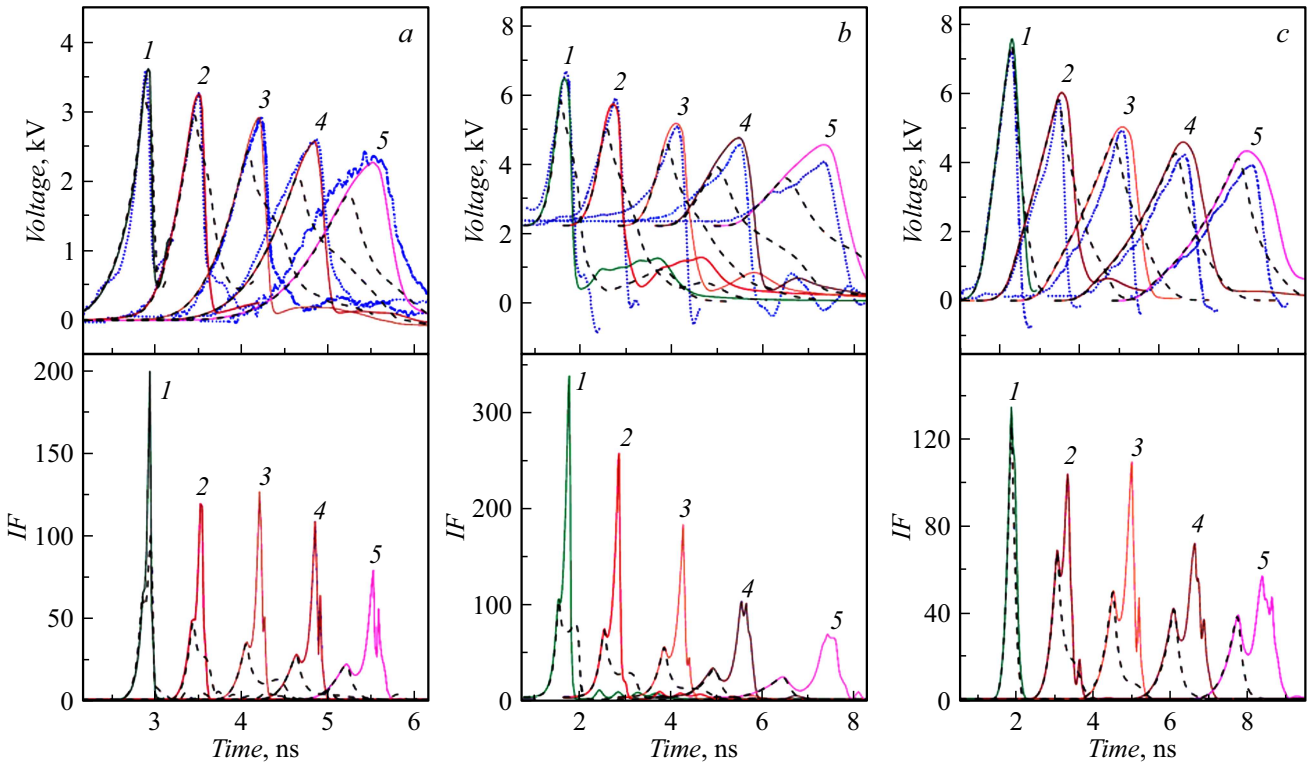

Figure 6. Comparison of experimental (dotted curves) and calculated (solid curves) dependences of voltage and integral factor IF on time during switching is shown in curves *1–5* for: *a* — silicon diode with diameter 6 mm with $\rho = 32\,\Omega\cdot$cm ($N_d \sim 1.5 \cdot 10^{14}\,\mathrm{cm}^{-3}$) at values of coefficient K, equal to 2.7, 4, 8, 12 and 30 without bias voltage [20]; *b* — silicon thyristor with diameter 32 mm with $\rho = 80\,\Omega\cdot$cm ($N_d \sim 0.6 \cdot 10^{14}\,\mathrm{cm}^{-3}$) at values of coefficient K, equal to 2.7, 4, 4.65, 10 and 15 with bias voltage; *c* — silicon thyristor, as in (*b*) at values of coefficient K, equal to 1.9, 3.5, 4.8, 7 and 10 without bias voltage. Dashed curves show calculated dependences at $K = 1.01$.

with plasma, and then p-base. Two „keys“ are processed in series, ensuring the observed in experiment linear voltage drop at switching stage. Operation of „keys“ critically depends on size of active area. If it exceeds definite limit, the current density is lower the value necessary to create field regions with amplitude above ionization threshold, and „key“ does not operate.

Switching the thyristor without applied bias voltage is performed similarly to above described, but there are some features. Calculation results of voltage and current through active part are shown in curves *3* and *4* in Fig. 4, distributions of carrier concentration and field for time moments in Fig. 4 are shown in Fig. 5, *b*. Voltage is applied to structure filled with basic carriers, so first of all in vicinity of n-p-transition SCR is created. Electrons and holes move to opposite sides from n-p-transition, as result SCR zone increases, and concentration of carriers decreases, until it will be below $106\,\mathrm{cm}^{-3}$ (curves *7* and *8* in Fig. 4). Width of n- and p-bases in thyristor structure of p^+-p-n-p-n^+-type is such that holes and electrons from regions of p-n- and p-n^+-transitions, respectively, have not time to reach SCR. So, further increase in concentration of holes and electrons (curves *7* and *8* in Fig. 4) is linked exclusively with processes of tunnel ionization of deep levels in region of strong field in SCR. When concentration $n_0 \sim 10^9\,\mathrm{cm}^{-3}$ is reached (shown by dashed line in Fig. 4) the processes of avalanche multiplication are activated, and further increase in carriers concentration is linked with this.

As SCR width increases its share in total voltage increases, and of neutral part of n-base — decreases. At time moment corresponding to maximum IF_1 in Fig. 4, the geometry of field distribution in structure of thyristor with and without bias voltage significantly differs from each other (curves *1* in Fig. 5, *a* and *b*). This is associated with fact that speed of carriers in neutral part of n-base saturates, and in field distribution the constant section appears. Area under the curve of field distribution in case of thyristor without bias voltage is larger than with it. Just with this the circumstance the observed in the experiment at $dU/dt > 4\,\mathrm{kV/ns}$ exceedance of switching voltage of thyristor without bias voltage relative to thyristor with bias is linked (Fig. 3). At $dU/dt < 4\,\mathrm{kV/ns}$ voltage on structure decreases, speeds of carriers in neutral part of n-base do not saturate, and pattern is changed to opposite one.

In thyristor with bias voltage relative to thyristor without it SCR width is larger, hence shock-ionization front edge passes larger distance, and field amplitude reaches larger values (Fig. 5). This results in higher density of excess plasma and shorter duration of the switching process in thyristor with bias voltage compared to thyristor without

it, which is in agreement with the experimental results (curves *3* and *4* in Fig. 3).

At $dU/dt > 8$ kV/ns in calculations e observe the change of source of initial carriers starting the switching process of the thyristor without bias voltage. Secondary holes occurred during ionization of the neutral part of *n*-base, enter SCR and start formation of shock-ionization front edge. This mechanism coincides with mechanism detected earlier in [31].

As calculations showed the distributions of concentration of carriers and field in place of shock-ionization front edge start depend on voltage increasing rate dU/dt, but not on value of applied bias voltage. At close values dU/dt, as it is seen from comparison of curves *1* in Fig. 5, *a* and *b*, they practically coincide. This circumstance is significant for analysis of spatial heterogeneity of the switching process and is studied in detail further.

2.3. Spatial heterogeneity of switching process

Fig. 6 presents calculation results of switching processes for silicon diodes and thyristors with and without bias voltage. The most close to experiment calculation dependences of voltage and integral factor IF on time are shown. For comparison the experimental dependences (dotted curves) and calculation results of practically homogeneous switching at $K = 1.01$ (dashed curves) are provided. It is obvious,that accounting of switching heterogeneity ensures to obtain good agreement with the experiment. Note also that with increase in increasing rate of acting voltage the calculation results of homogeneous switching approach the experiment, i.e. degree of switching process homogeneity increases (see curves *1-5*).

In dependences of ionization intensity on time presented in form of integral factor IF in Fig. 6 there are three characteristic maxima (IF_1, IF_2 and IF_3 in designations in Fig. 4), which relate to the process of formation of shock-ionization front edge in SCR, process of filling with plasma of *n*-base and regions beyond it. When dU/dt increases the first maximum shifts to second one until it merges with it. In this case, the moments of the start of the shock-ionization front edge and the beginning of the switching process coincide, and the switching process itself becomes practically homogeneous.

As Fig. 6 hows, during transition from curve *5* to curve *1* the voltage increasing rate increases, hence, the we observe increase in voltage value and field amplitude reached in the device structure during formation of shock-ionization front edge. This results in increase in the intensity of ionization process in structure and amplitude of first maximum of integral factor IF_1 in curves *5-1* in Fig. 6.

During homogeneous switching ($K = 1.01$), presented as dashed curves in Fig. 6, maximum IF is always one and coincides with maximum IF_1 of heterogeneous switching. During heterogeneous switching the start of shock-ionization front edge results in current redistribution in the device: current through the active part increases, and through passive part — decreases. Respectively voltage and intensity of ionization processes in active part increase until density of generated electron-hole plasma will be sufficient to compensate the field in the device structure and start of voltage decreasing. During spatial-homogeneous switching such current redistribution does not occur, and after start of shock-ionization front edge the current through the structure and voltage on it start decreasing immediately. As the obtained at that dependence of voltage on time significantly differs from the experimental one, then we can suppose that the spatial heterogeneity exists already at time of start of shock-ionization front edge.

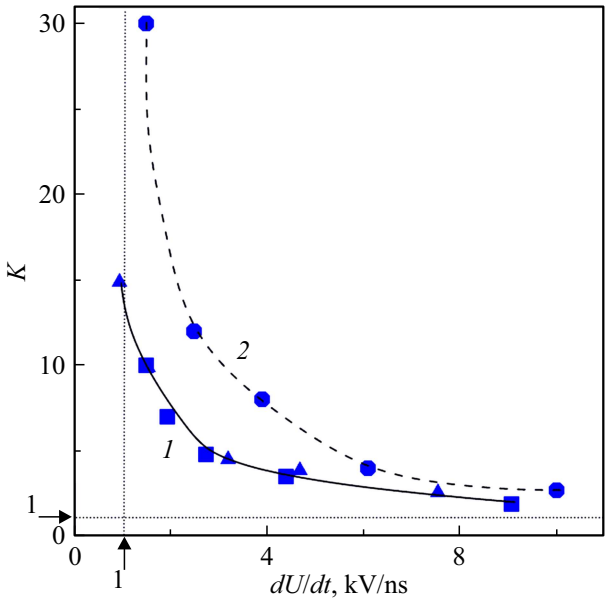

Figure 7. Dependence of coefficient K (S/S_a) ob increasing rate of switching voltage for silicon diode with diameter 6 mm with $\rho = 32\,\Omega\cdot$cm (circles) [20], for silicon thyristor with diameter 32 mm with $\rho = 80\,\Omega\cdot$cm with applied bias voltage (triangles) and without it (squares).

Based on the results of comparison of calculations and experimental data shown in Fig. 6, it is possible to make dependencies of the value $K = S/S_a$ on increasing rate of switching voltage dU/dt.

Dependences for switching of silicon diodes and thyristors with and without pre-applied bias voltage are shown in Fig. 7. We see that upon decrease in dU/dt value K quickly increase which corresponds to decrease in size of active area until its complete disappearance at $dU/dt < 1$ kV/ns. This result is in good agreement with the experimental fact of presence of the effect of quick switching at $dU/dt < 0.5$ kV/ns [17]. When dU/dt increases the value K monotonically tend to 1 which equivalent to active area approaching to total area of the device.

As previously in [18], the decrease in resistivity of the device material results to increase in K at fixed dU/dt (curves *1* and *2* in Fig. 7). When resistance of semiconductor material increases the electric field distribution

in structure becomes more homogeneous, and volume of region occupied by processes of avalanche multiplication increases. And though the field amplitude decreases, the total number of places where current channels arise, constituting the active area, increases.

Calculations showed that size of active area during switching the thyristor depends on voltage increasing rate dU/dt, but not on whether bias voltage was applied or not (triangles and squares in Fig. 7). The process of formation of shock-ionization front edge in SCR also does not depend on bias voltage: intensity of ionization processes and concentration of carriers at moment of front edge formation are determined only by value dU/dt (curves *1* in Fig. 5). On other hand, to agree with the experimental data it is necessary that the heterogeneity of the current distribution over the device area be present in the device structure already at the stage of formation of the shock-ionization front edge. These circumstances ensure supposition that size of active area depends on intensity of ionization processes at moment of formation of shock-ionization front edge, i.e. on value IF_1. Using results in Fig. 6 we prepare (Fig. 8) the dependence of ratio of active and total areas on value IF_1 for switching the thyristors and diodes with pre-applied bias voltage and without it. Two additional points (light circles in Fig. 8) were obtained using calculations of the switching process for diode at higher, then in experiment, increasing rates of switching voltage — 25 and 17 kV/ns, corresponding to them sizes of active area — 0.55 and 0.63 — were obtained by interpolation of curve *2* in Fig. 7. From Fig. 8 we see that all points lie along one curve, and upon change in value IF_1 from 20 to 180 the portion of active area increases from 0 to 0.8 of total area of device. Note that spatial heterogeneity exists only in limited range of value IF_1 change. At that making the dependence of active area on maximum IF_2 or average over time value IF does not permit obtaining of the uniform curve for all points. So, If we use as the parameter not the avalanche multiplication coefficient but its integral, then all points lie along one curve regardless of the device structure (diode or thyristor), the resistivity of the material and the magnitude of the pre-applied voltage.

Dependence shown in Fig. 8 is limited by value $IF_1 \sim 20$, below which the active part disappears. Value $IF_1 \sim 20$ corresponds to minimum intensity of ionization processes, which ensures generation of electron-hole plasma with concentration equal to level of base doping. This is a necessary condition for compensating the electric field created by dopant ions and start of the shock-ionization front edge. At $IF_1 < 20$ shock-ionization front edge is not formed, and the switching process occurs more slower due to shock ionization avalanches movement with saturated speed. Note that condition $IF_1 < 20$ correlates to the condition $dU/dt < 1$ on Fig. 4, when the active area decreases to zero, and with observed in experiment disappearance of the effect of quick switching at $dU/dt < 0.5$ kV/ns [17].

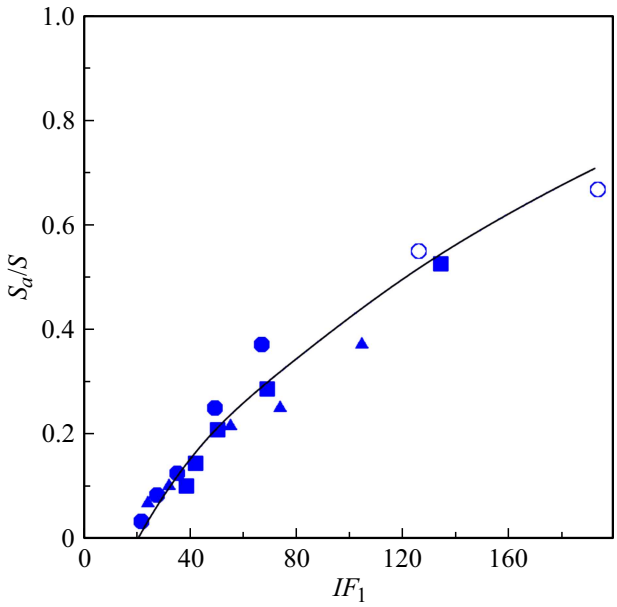

Figure 8. Ratio of active and total areas vs. amplitude of first maximum of integral factor IF_1 for silicon diode with diameter 6 mm with $\rho = 32\,\Omega$·cm without bias voltage (circles) [20] and silicon thyristor with diameter 32 mm with $\rho = 80\,\Omega$·cm with applied bias voltage (triangles) and without it (squares). Light circles — see explanations in text.

Conclusion

In paper we studies experimentally and theoretically the process of thyristor switching by voltage pulse increasing with rate dU/dt below 10 kV/ns. The thyristor has structure of p^+-p-n-p-n^+-type 520 μm thick and 32 mm in diameter, and was made of silicon with $\rho = 80-85\,\Omega$·cm. Studies were performed both in mode with pre-applied bias voltage ($U_0 = 2.2$ kV), and without it. In calculations we assume that the device area is divided into active part, where ionization processes occur, and passive part without them. According to calculation results sizes of active area S_a were determined to ensure best coincidence of calculated and experimental voltage oscillograms. For characterization of the ionization processes intensity in calculations the integral factor IF was introduced, it was equal to number of electro-hole pairs arising due to the processes of avalanche multiplication when single carrier passes through region of strong electric field. Let's discuss the obtained results.

Firstly, upon dU/dt increasing from 1 to 10 kV/ns the switching voltage increases from 3 to 7 kV, and switching process duration decreases to 200 ps. At $dU/dt < 4$ kV/ns the thyristor with bias voltage as compared to the thyristor without it has lower duration of the switching process and higher amplitude of switching voltage. At $dU/dt > 4$ kV/ns the switching voltage of thyristor without bias becomes higher then of thyristor with bias. The calculations show that this is linked with field amplitude increasing in structure and saturation of movement speed of carriers in neutral part

of *n*-base, as result the constant section appears in the field distribution.

Secondly, duration of the switching process at $dU/dt \sim 1$ and 1.5 kV/ns start to increase asymptotically with applied bias and without it, respectively. These values are close to value dU/dt, below which the effect of quick switching disappears in earlier performed experiments [17].

Thirdly, the calculations well describe the experimental results only at definite type of dependence S_a on dU/dt. Value S_a increases with increase in dU/dt approaching the total area of device at $dU/dt > 10$ kV/ns. With dU/dt decreasing the value S_a decreases, tending to zero at $dU/dt < 1$ kV/ns. it is determined that switching mode of thyristor both with bias voltage and without it does not affect the dependence S_a on dU/dt.

Fourthly, spatial heterogeneity of current distribution along the area occurs at stage of shock-ionization front edge formation in SCR of device. Size of active area is proportional to the intensity of ionization processes at this stage, its characteristic is value of maximum of integral factor IF_1. All points in dependence S_a on IF_1 lie along one curve, and upon change in value IF_1 from 20 to 180 the value S_a increases from 0 to 0.8 of total area of device (Fig. 8). Conditions of active area disappearance $IF_1 < 20$ and $dU/dt < 1$ kV/ns are equivalent to each other and close to the experimental limit of switching effect. The condition $IF_1 > 180$ corresponds to $dU/dt > 10$ kV/ns, when value S_a practically becomes equal to total area of the device, and start of shock-ionization front edge occurs simultaneously with start of switching process.

Fifthly, for wide analysis we use data on switching the power diodes [20]. Uniform dependence S_a on IF_1 is obtained for diodes and thyristors regardless of the semiconductor material resistance and values of bias voltage.

Paper shows that there is correlation between active area and intensity of ionization processes at stage of shock-ionization front edge formation in SCR of device. Nature of active area at this stage, apparently, is linked with spatial heterogeneity of field distribution and discrete nature of avalanches occurrence. At time of start of shock-ionization front edge the current along its area is also distributed inhomogeneously. Upon front edge movement only increase of heterogeneities is possible [11]. Places of front edge reached border of SCR first form the channels with high conductivity, as result current redistribution in them occurs in their favor. Area of these channels is actual active area through which current flows further during switching Value S_a, determined from comparison of calculation and experiment, is parameter which is evaluation of average actual active area.

Existence of spatial heterogeneity of current distribution along the device area is a rather coarse effect, as upon change in dU/dt from 1 to 10 kV/ns size of active area increases from zero to practically total area of device. Such large change of active area can not be explained by incorrect measurements and by model assumptions. At $dU/dt < 10$ kV/ns spatial heterogeneity is integral feature of the effect of quick (picosecond) switching. This, in particular, permits description of the experiment, during which the effect of quick switching was determined [1], as spatial heterogeneous switching under action of shock-ionization waves. If heterogeneity is not considered, the calculated duration of the switching process is overestimated by several times relatively to experimental one (see dashed curves in Fig. 6, *a*).

As the dependence between the size of active area and value IF_1 is obtained base on t=rather general considerations, we can expect that similar dependence will be observed at some change in temperature also in other semiconductors, where the effect of quick switching is determined.

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Conflict of interest

The authors declare that they have no conflict of interest.

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