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Field-effect transistor with graphene channel and epitaxial calcium fluoride layer as a gate dielectric

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The samples of field-effect transistors for two-dimensional electronics using a combination of graphene (as a channel material) and epitaxial calcium fluoride (as a gate-insulating material), have been fabricated for the first time. Conventional measurements of terminal currents in these devices confirmed their functionality. The study can be treated as a step toward creation of the scalable transistors with the new promising materials. One of the nearest challenges is reduction of the sample-to-sample spread of the characteristics.

Keywords: 2D electronics, field-effect transistor, graphene, calcium fluoride.

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The most important area of the microelectronics development of today is the search for new materials for the fabrication of its basic elements — metal-insulator-semiconductor field-effect transistors (MISFET). Usually, the reference publications are concentrated on the selection of semiconductors, which, in the course of miniaturization, could substitute conventional Si. The promising ones include two-dimensional, 2D materials [1,2], such as graphene, silicene and transition metals dichalcogenides. In the recent decade, the transistors with a current-carrying layer (channel) were created from such materials [1,2]. Among 2D-materials, graphene is especially interesting because of a high mobility of the charge carriers. At the same time, unlike dichalcogenides, which are potentially interesting for digital electronics applications, graphene has zero band gap, so the solid-state optoelectronics and sensorics seem as the primary scope of application of transistor structures based on it.

Possible design option for that transistor is shown in Fig. 1. The design itself is not innovative, however, the combination of graphene–fluoride is introduced by us in such devices for the first time. In the design presented, the function of the gate refers to lower electrode, the voltage V_g on it controls the value of the current I_d from the source to drain. Here, the function of silicon is virtually „mechanical“ since the significant processes take place not in Si, but in the conducting 2D-layer located on the dielectric.

Certainly, along with the optimization of selection of semiconductor 2D-film, the selection of a dielectric plays a great role, because it will define the stability of functioning of the device as a whole (parasitic recharging phenomena in the dielectric could have an effect), the mobility of electrons and holes in the channel, as well as possible range of operating voltages. Conventional silicon dioxide (SiO_2) and high-k-oxides (HfO_2, Al_2O_3, etc.) are still applied in the electronics for the type of transistors in question [3]. However, as it was established, neither SiO_2, nor „alternative“ amorphous oxides provide a satisfactory quality of the insulator–conducting channel interface, thus disabling the advantages of the use of 2D-material [3]. An option of application of crystalline hexagonal boron nitride (hBN) was tried, giving a good result, but, firstly, dielectric properties of that material leave much to be desired [3], and, secondly, unpractical high-temperature regimes are required for its deposition [4].

In the present work we fabricated for the first time graphene-based 2D-transistors using completely different dielectric — calcium fluoride (CaF_2) (Fig. 1). CaF_2 is relatively poorly known as a material for microelec-

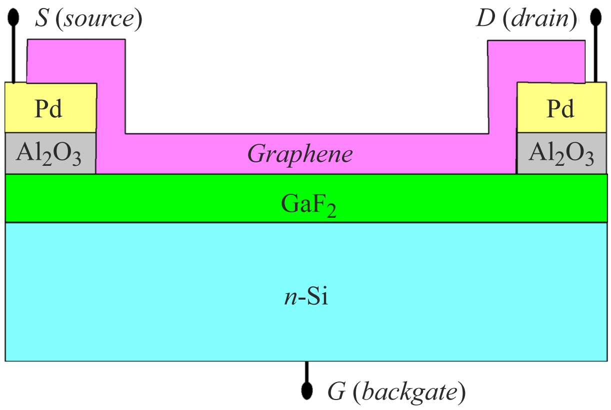

Figure 1. The structure of the studied field-effect transistor. The graphene film serves as a current-conducting layer, and fluoride — as a gate insulator (earlier, other combinations of materials were used in such devices: MoS_2/hBN/Si, etc.).

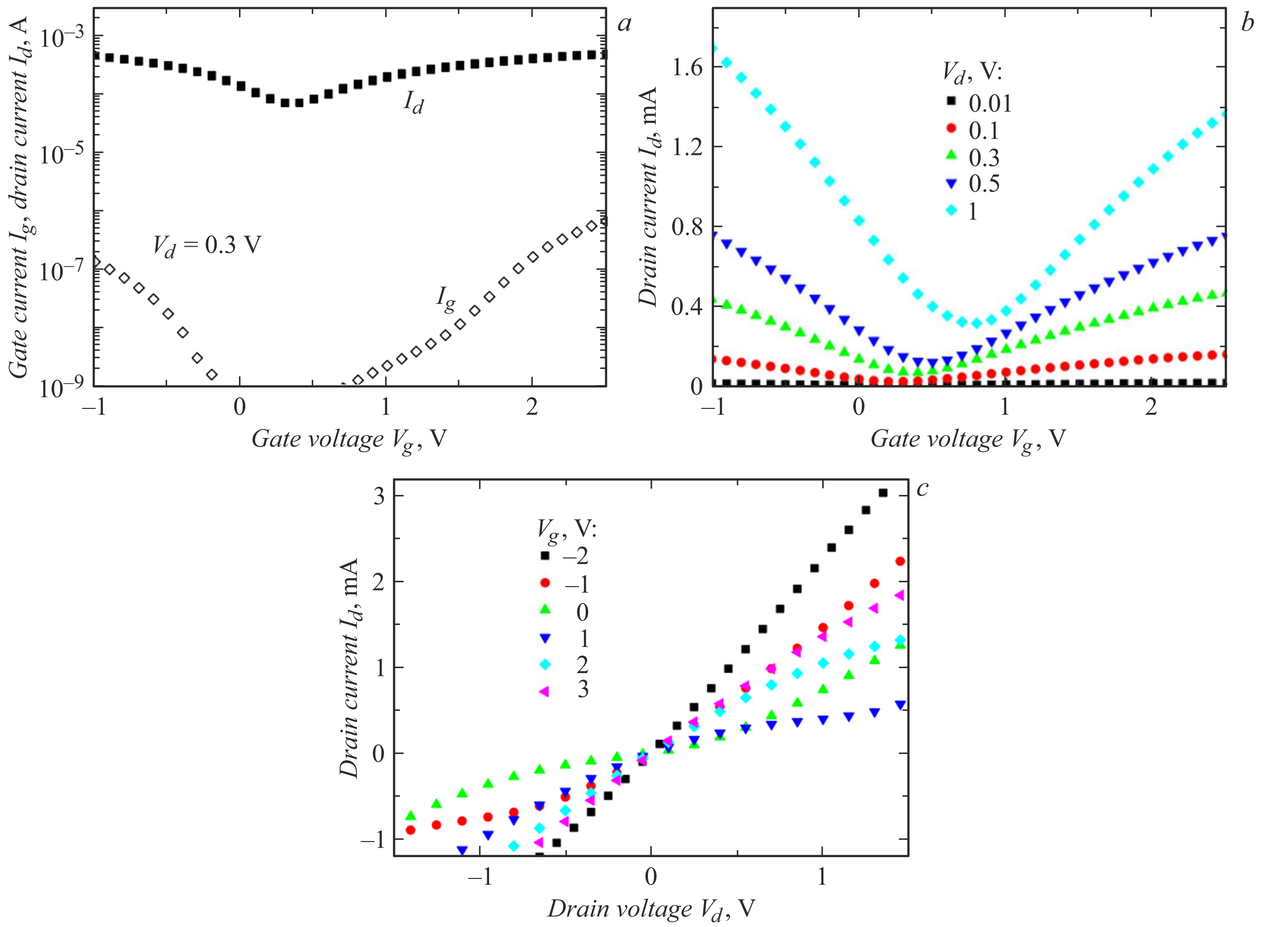

Figure 2. Typical characteristics of transistors with graphene over CaF_2. *a* — comparison of the drain current and the leakage current through insulator; *b* — dependencies of the drain current on the voltage at the gate for several given drain voltages; *c* — dependencies of the drain current on the drain–source voltage for several given voltages of the gate. For all parts of Figure, the size of the channel is $L \times W = 80 \times 50\,\mu$m, the temperature is 25°C.

tronics. It was considered mainly as a candidate for barrier layers in resonant-tunneling diodes [5]. Its advantages are: a wide band gap ($E_g = 12.1$ eV), quite high dielectric permittivity (statically in statics $\varepsilon = 8.43$ [6]) and a good matching of the lattice constants CaF_2 and Si [5], enabling to grow single-crystal layers of that fluoride on the silicon by molecular-beam epitaxy. In different times, the application of CaF_2 in MISFET with simple architectures based on silicon, diamond and gallium arsenide was considered (see, e.g., [7]). In our earlier works we succeeded in creating 2D-transistors with the channel made of MoS_2 above the CaF_2 and in demonstrating that their characteristics in some aspects are superior to those of the similar devices with known dielectrics [8].

Therefore, this work is about trying to extend the experience we have gained for the 2D devices. A physical factor we hope to bring improvement is the formation of quasi-Van-der-Waals interface CaF_2–2D-material, which is to improve the channel characteristics.

Fabrication of the transistor structures studied herein included two key processes: growing the layer of CaF_2 with the nominal thickness of 2 nm and application of graphene, as well as auxiliary operations.

The layer of CaF_2 was formed by molecular-beam epitaxy on moderately doped substrates of *n*-type Si ($N_D = 10^{15}\,\mathrm{cm}^{-3}$) of orientation (111) with the miscut angle not more than 10 arcmin. After standard chemical treatment by Shiraki method [9], according to which a thin layer of oxide was chemically grown and removed multiple times, the finish layer of silicon oxide was thermally formed under the conditions of a ultra-high vacuum, after which epitaxial growth of CaF_2 was started at the deposition rate of ~ 1.3 nm/min. An optimum one was the growth temperature 250°C without post-annealing. Crystalline quality was controlled by the reflection high-energy electron diffraction pattern (RHEED, energy of 15 keV). The nominal thickness of the fluoride layer was about 2 nm, and its spatial inhomogeneity when assessed by the rms parameter was about 0.2 nm and tended to decrease as far as the nominal fluoride thickness is decreased.

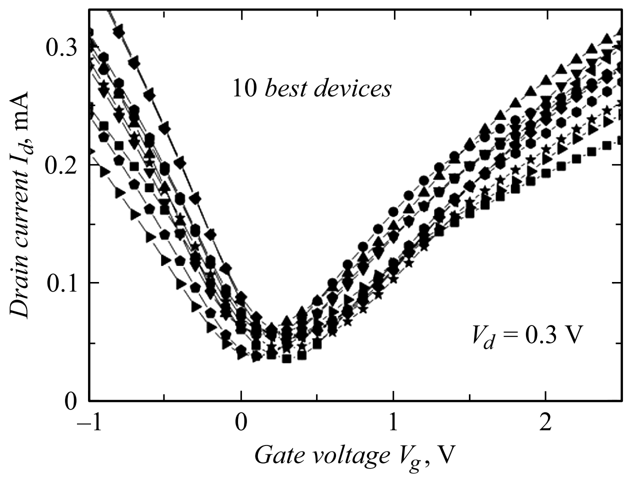

Figure 3. The characteristics of the best ten (out of about 50) devices demonstrating their relatively low spread.

The regions of drain and source terminals were formed above CaF_2 with application of photolithography: 10-nanometer sublayer of Al_2O_3 with palladium metallization. Graphene film, which was grown by chemical vapor deposition, was transferred to the formed structure; polymethylmethacrylate was used during the transfer. The channel size (length $L \times$ width W) was from 160×100 to $9 \times 3\,\mu$m. The function of „gate", as indicated before, was performed by the back terminal to the silicon substrate (backgate configuration).

Fig. 2, $a-c$ represents typical measured characteristics of the transistor with the size of $80 \times 50\,\mu$m: drain I_d and gate I_g currents as the functions of voltage at the gate V_g, as well as the drain current depending on the voltage of gate–source V_g (for the series of voltages at the drain) and drain–source V_d (for the series of voltages at the gate). In general, these characteristics indicate the functional capability and good control of the device. Thus, it is obvious from Fig. 2, a, that the leakage current I_g is far lower than the main current I_d, while, as easily verified through the division by the area $L \times W$, the gate leakage current density is several orders lower than 1 A/cm^2. Fig. 2, c shows apparent change of the current sign I_d during transition through zero for the drain voltage V_d. The drain current vs. gate voltage characteristics in Fig. 2, b clearly demonstrate controllability, namely, a pronounced dependence of the curves pattern on V_d and V_g, while position of the $I_d(V_g)$ curve minimum is shifted to the right with the increase of the positive voltage V_d, as it must be.

In the work we measured about 50 samples. In terms of quality, all of them demonstrated the expected characteristics. At the same time, at this stage of study a group of samples with low sample-to-sample differences in the current values was clearly distinguished (Fig. 3). A fraction of the devices, whose characteristics are arranged in the group, was about a quarter of the studied ones (ten curves were drawn for illustration), which indicates an adequate repeatability of the obtained functional transistors in the first experiments. It should be noted that ordinate axis in Fig. 3 is not logarithmic, i.e. the spread within the „best" group does not exceed two times for the current. We suppose that apparent quantitative deviations from the characteristics in that group are associated with the defects in certain samples.

We may conclude, that during the work we obtained 2D-transistors based on graphene and calcium fluoride combination for the first time. This combination of materials was not considered earlier for 2D-devices.

Assessing the result, one should note that we have not done the process optimization yet, though there is an obvious potential for that. In particular, it seems to be real to achieve higher homogeneity of the fluoride layer, which will reduce the spread. The channel protection from the top will also contribute into it. In perspective, one shall not exclude also the use of other similar fluorides or their solid solutions. One of the steps in the nearest future shall be systematic comparison of advantages and disadvantages of the graphene/CaF_2/Si structures with the case of using more common dielectrics (SiO_2, hBN).

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Conflict of interest

The authors declare that they have no conflict of interest.

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