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Multilevel memristor structures based on a-Si with enhanced resistive switching stability and low compliance currents

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Using the magnetron deposition and thermal sputtering techniques, we synthesized the Cr/Cu–Ag/a-Si/natural oxide SiO_x/p^{++}-Si structures with enhanced resistive switching stability (more than 10^4 write/erase cycles), which is several orders of magnitude higher than previously reported. At the same time, the structures demonstrate the multilevel character of switching at compliance currents of up to 1 μA and have the retention time of resistive states of at least 10 min. A possible mechanism for the formation of stable resistive switching is discussed.

Keywords: memristors, a-Si, magnetron deposition, multilevel resistive switching, low compliance currents.

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The memristive effect is associated with variation in the resistive state of the object (memristor, that is, a resistor with memory) under the action of the applied electric field and a charge passing through it, and also with retention of this state after removing the voltage pulse. Memristors are quite promising elements for constructing a new-type non-volatile random-access resistive memory like RRAM and neuromorphic computing systems because they can possess low energy consumption for data write/read operations and multilevel resistive switching (RS), and, therefore, are able to emulate key elements of neuromorphic computing systems, namely, synapses [1–8].

At present, of the highest interest are memristor structures of the metal–dielectric–metal (MDM) type as they are systems able to exhibit the multilevel character of RS at long times of the resistive state retention, and also are technologically simple and may be easily integrated into the up-to-date silicon microelectronic technologies [1–3]. Therewith, the most widely used techniques for creating MDM-memristors are magnetron sputtering, atomic-layer deposition and various types of chemical vapor deposition (PECVD, MOCVD) [9], since they enable obtaining large-area high-quality dielectric and metal coatings compatible with conventional procedures for creating CMOS chips.

Impressive success in developing scalable memristors with quasi-analog RS were demonstrated in [10] where the effect of RS was studied in the Cu–Ag/a-Si/p^{++}-Si structures based on thin (5 nm) layers of amorphous silicon (a-Si). Multilevel RSs observed in this system were explained by electromigration from the composite Ag–Cu electrode of mobile Ag atoms and even more mobile Cu atoms inclined to form silicides and stabilizing the generated Ag–Cu „alloy" metal nanobridges [10]. However, the demonstrated stability in the cycles of switching from the high-resistance state (off) to low-resistance state (on) and back (in other words, in the write/erase cycles) appeared to be quite poor (~ 100) though during quasi-continuous transitions between the „off" and „on" states the number of RS cycles exceeded 10^5. A certain disadvantage of the Cu–Ag/a-Si/p^{++}-Si structures consists in considerable RS limit currents I_c (compliance currents) exceeding 1 mA. However, undoubtful advantages of the structures developed in [10] are the formless character of RS, scalability, and possibility of creating an array of matrix memristors in the dense crossbar architecture compatible with the Si-technology (paper [10] has shown the possibility of creating passive matrices 32×32).

Another case of implementing large arrays of memristor matrices was demonstrated using as an example the Au–Ag/i-SiO_x/p^{++}-Si structures based on natural (native) oxide SiO_x (hereinafter referred to as i-SiO_x) [11]. It turned out that i-SiO_x 2–3 nm thick has rather homogeneous properties that allowed the authors of [11] to demonstrate a quite low RS variability of the structures both from cycle to cycle (1.1%) and from device to device (2.6%). High RS stability of the structures ($> 5 \cdot 10^5$ cycles) was also demonstrated. However, such structures needed electroforming (voltages of up to 6 V), which manifests itself as a disadvantage in the process of integrating them into modern CMOS chips whose operating voltage is < 3 V. In addition, the structures required for rather high RS limit currents $I_c = 1-10$ mA [11].

One of the approaches to stabilizing RS of the MDM structures, which are under development at present, involves introducing into their active regions extra (barrier) layers preventing motion of ions [12]. In this study, an attempt was

undertaken to perform such a stabilization in the a-Si-based structures by introducing an i-SiO$_x$ barrier layer between the layer of a-Si and p^{++}-Si substrate (electrode); this layer can additionally reduce limit currents I_c during RS.

For this purpose, structures Cr/Cu−Ag/a-Si/i-SiO$_x$/p^{++}-Si were synthesized by magnetron deposition and thermal sputtering. As the substrate and lower contact, wafers of degenerate crystalline (100) silicon (p^{++}-Si) doped with boron and having specific resistance of $0.001-0.005\,\Omega \cdot$ cm were used. Prior to producing a layer of fresh natural oxide, organic and non-organic contaminations, as well as the existing layer of i-SiO$_x$, were removed from the wafer surfaces using Caroś acid and hydrofluoric acid. After that, the wafers were rinsed with deionized water and dried in the isopropyl alcohol vapors.

To create a layer of fresh i-SiO$_x$ 2−3 nm thick, the Si wafers were kept for a week in a closed container under the environmental conditions at the atmospheric pressure and room temperature. Then the a-Si layer 5 nm thick was deposited by direct-current magnetron sputtering (DC mode) of an undoped pure-Si (99.999%) target (made on a copper substrate produced by „Kermet“LLC). The target diameter was 4”, sputtering power was 800 W, duration was 3 min, argon pressure was $3 \cdot 10^{-3}$ Torr. After that, the upper Cr/Cu−Ag electrode 0.5×0.2 mm in size was formed. First the Cu−Ag alloy film 15 nm thick was created by thermal sputtering; then the Cr layer 300 nm thick was fabricated by magnetron deposition. To obtain the Cu−Ag-alloy film by thermal sputtering, there was used a sample weight of 4.55 mg of Ag and 3.82 mg of Cu (corresponding to the composition of the 50/50 vol.% copper/argentum alloy). The layer of Cr was fabricated at the following performance parameters: deposition time of 15 min, argon pressure of $3 \cdot 10^{-3}$ Torr, DC-source sputtering power of 1000 W.

The volt-ampere (I-V) characteristics of the structures and effects of resistive switching were studied at room temperature by using a multipurpose sourcemeter KEITHLEY 2636B and analytical probe station SWIN EPS4. The I-V characteristics were measured in the mode of limit current with the earthed lower electrode of the structures and with the upper electrode bias voltage increasing according to the linear-stepwise law in the $0 \to +6 \to -6 \to 0$ V sequence with the step of 0.1 V and step length of 50 ms. The number of sweep cycles, as well as the step amplitude and duration, were set programmatically.

Experiments have shown that the structures possess stable RS with the ratio between resistances in the high-resistance and low-resistance states (R_{off}/R_{on}) of up to 10^3. The RS limit currents amount up to $I_c = 0.1$ mA (Fig. 1).

The number of possible RS states was determined by varying the RS voltage in the range from 3 to 3.5 V at the limit current of $I_c = 1\,\mu$A. The experiments revealed four stable states retainable for more than 10 min (see Fig. 2). In those experiments, the states were read by applying to the structure voltage pulses 1 V in amplitude and 50 ms in duration.

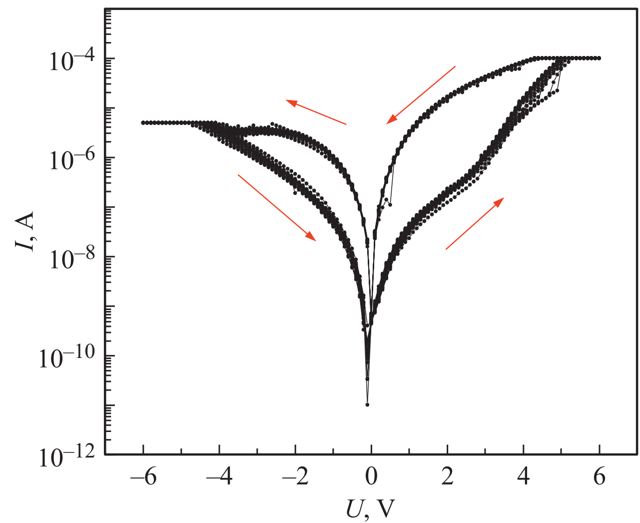

Figure 1. I-V characteristics of the Cr/Cu−Ag/a-Si/i-SiO$_x$/p^{++}-Si structure measured at the limit current of $I_c = 0.1$ mA and upper contact area of 0.25×0.2 mm. Arrows indicate the directions of voltage sweeping for different branches of I-V characteristics.

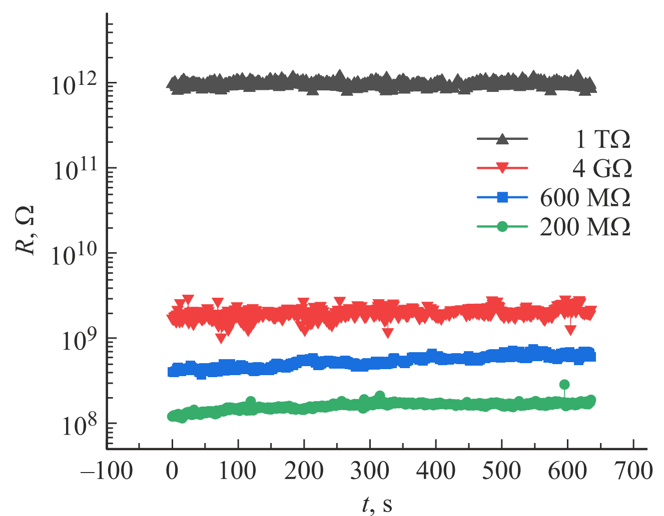

Figure 2. Time dependences of the structure Cr/Cu−Ag/a-Si/i-SiO$_x$/p^{++}-Si resistance in different resistive states (retention).

The structures were studied for resistance to degradation during resistive switching (endurance) by sequentially applying voltage pulses 50 ms in duration: $U_{set} \to U_r \to U_{reset} \to U_r$, where $U_{set} = +2.5$ V is the „write“ voltage converting the structure to the low-resistance state, $U_r = 0.1$ V is the „read“ voltage , $U_{reset} = -2.5$ V is the voltage of „erase“ (reset) or the structure return to the initial state. The number of switchings between the R_{off} and R_{on} states in the structure under study exceeds 10^4 (Fig. 3, a).

We associate the revealed stable resistive switching of the Cr/Cu−Ag/a-Si/i-SiO$_x$/p^{++}-Si structures at relatively low limit currents $I_c \leqslant 0.1$ mA with the fact that the Cu diffusivity in Si is two orders of magnitude higher than

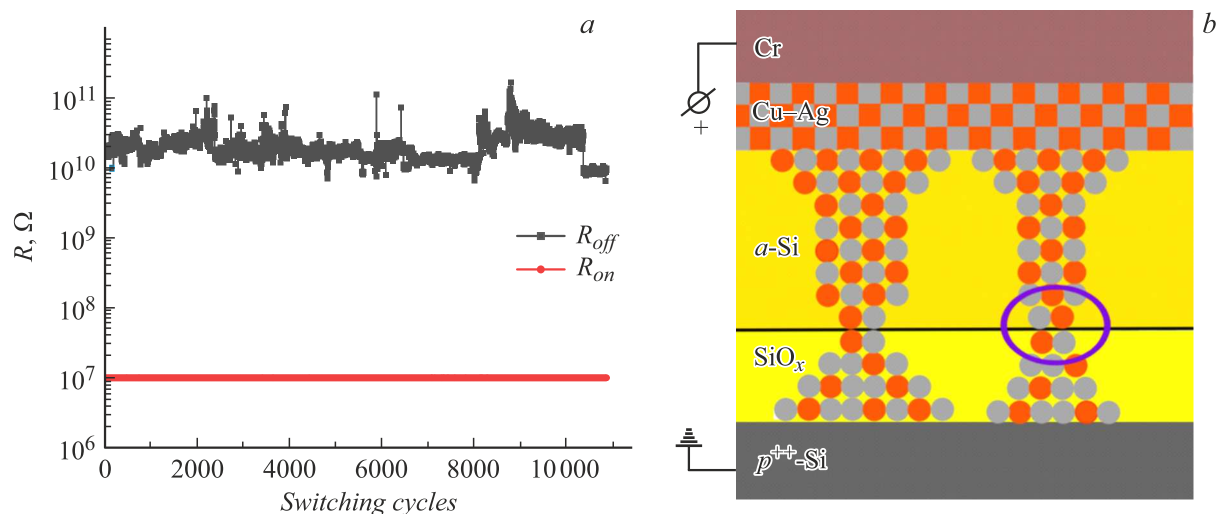

Figure 3. a — electric resistance of the Cr/Cu–Ag/a-Si/i-SiO_x/p^{++}-Si structure versus the number of the write/erase cycles (cyclic RS stability — endurance). b — schematic representation of the Cr/Cu–Ag/a-Si/i-SiO_x/p^{++}-Si structure in the mode of resistive switching to low-resistance state R_{on}. Gray symbols correspond to Ag, red ones are for Cu. The oval curve marks the place of RS. The colored figure is given in the electronic version of the paper.

that in SiO_2, while the respective diffisivities of Ag are approximately equal to each other [13,14]. As a result, according to the model proposed in [10], „thickened" electrically durable alloy nanowires Cu–Ag get formed, which determine positions of RS areas in i-SiO_x. To our mind, fixation of the RS areas near the a-Si/i-SiO_x interface (Fig. 3, b) is just that causes the enhancement of RS stability of the developed structures similarly with the case of RS of nanocomposite-based structures in the mode of multifilament switching [15]. It is important to notice that RS limit currents decrease significantly in the case under consideration.

Thus, in this work structures Cr/Cu–Ag/a-Si/i-SiO_x/p^{++}-Si based on amorphous silicon and its natural oxide were synthesized using magnetron deposition and thermal sputtering; the structures possessed stable multilevel resistive switching at compliance currents which were more than an order of magnitude lower than those in the structures based on a-Si [10] or i-SiO_x [11]. The obtained results demonstrate hopeful prospects for employing the developed memristive structure in creating energy-efficient neuromorphic computing systems and can promote further progress in the proposed technology.

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Conflict of interests

The authors declare that they have no conflict of interests.

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