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Measuring the mobility of charge carriers in samples with low conductivity by the field effect transistor method using output characteristics

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FET-based charge carrier mobility measurements in low-conductivity materials, as well as semiconductor materials with a high density of trapping states, such as nanocrystals and polycrystalline films, are highly distorted due to charge accumulation in the transistor structure. In this work, a comparative study of the measurement of the mobility of charge carrier in conductive polymers, nanocrystals and polycrystalline films, using the analysis of output and transfer characteristics, was carried out. It is shown that using output characteristics instead of transfer characteristics for calculating the charge carrier mobility helps to avoid a systematic error in the measurement.

Keywords: field-effect transistor, FET, charge carrier mobility, output characteristics, transfer characteristics, charge accumulation, nanocrystals.

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Introduction

The field-effect transistor method is widely used to measure the mobility of charge carriers by determining the steepness of the drain-gate characteristic, i.e. the dependence of the current in the channel on the voltage at the gate $I_{\mathrm{DS}}(U_{\mathrm{GS}})$. For the linear mode the mobility is defined as [1]

$$\mu_{\mathrm{lin}} = \frac{L}{WC_{\mathrm{ox}}V_{\mathrm{ds}}} \left.\frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{gs}}}\right|_{V_{\mathrm{ds}}=\mathrm{const}},$$

where W is the channel width, L is the channel length, C_{ox} is the insulator layer capacitance per unit area (oxide capacitance), μ is the mobility. The measurement method is described in detail in [2,3]. In addition, the structure of the field-effect transistor is used in sensors, where the reaction of the channel material (for example, graphene) with the analyte leads to a change in the response of the transistor to the gate voltage [4]. By itself, the method of studying mobility using field-effect transistors is characterized by a large number of factors that can affect the final result and require attention in the study [5]. Moreover, in the case of studying materials with low conductivity and prone to the formation of trap states, these results are strongly distorted, and in some cases they cannot be obtained at all [6]. This is especially common in the study of nanocrystal (NC) films due to the large surface-to-volume ratio, which leads to a large number of surface defect states. These states are charged by the flowing current, which leads to screening of the channel material from the gate field, as well as charging the gate itself as the second plate of the capacitor. When the gate voltage changes, which is required to obtain a drain-gate curve, the charge accumulation in the transistor structure becomes a dynamic process and turns out to be the main cause of current flow in the channel, if the conductivity of the material under study is low and the expected current is nanoamperes. Such a process is easy to detect, since it is accompanied by the appearance in the gate electrode of a current comparable to the current in the channel. This current is the charging current of the capacitance formed by the gate and channel separated by an insulator layer [3].

Since the main problem in obtaining drain-gate characteristics is the accumulation of charge in the transistor structure as the gate voltage increases, the mobility estimate from a series of drain (output) dependencies $I_{\mathrm{DS}}(V_{\mathrm{DS}})$ obtained at different gate voltages V_{DS} seems to be more reliable, since when they are obtained, charge accumulation occurs once, when the gate voltage is turned on, after which the degree of charge influence on measuring the current I_{DS} in the channel does not change (although the charging of the capacitance itself can make a constant correction for the channel conductivity). Comparison of the results obtained in two different ways can also provide additional information about the object under study, namely, the presence of charging trap states in the active layer or at the interface between the active layer and the insulator. In addition, in some cases, changing the method can provide an increase in the sensitivity of sensors based on field-effect transistors.

In this paper, we analyze data obtained using the field-effect transistor method for a number of materials widely used in the fabrication of multilayer photovoltaic devices, both as active and auxiliary (electron-transport and hole-transport) layers: a conductive polymer (PEDOT:PSS), semiconductor NCs of zinc oxide (ZnO) and lead sulfide (PbS), as well as a polycrystalline semiconductor with a perovskite structure ($MAPbI_3$). Obtaining data on the

mobility of charge carriers in these materials is important for the further development of optoelectronic devices. Two schemes for creating a field-effect transistor are used and the difference in the results of measuring the mobility of charge carriers obtained from drain and drain-gate characteristics is shown.

1. Review

The phenomenon of charge accumulation in a semiconductor field-effect transistor is well known. It is caused by the formation of charges in the volume of the dielectric, as well as surface states at interphase boundaries, and leads to a change in the threshold turn-on voltage, and also affects the slope of the current-voltage characteristics of the transistor [7]. The phenomenon of transistor structure charging, which makes it impossible to study the mobility of charge carriers in thin NC films, has been repeatedly mentioned in the literature. Thus, Ref. [6] describes the study of the effect of air on layers of PbSe NCs with a diameter of 6−8 nm, coated with a 1,2-ethanedithiol (EDT) ligand shell. In the NCs, after exposure to air, with a stepwise change in the gate potential, the current strength quickly returns to its previous value (in a few seconds), as if the gate field was completely screened by the charges in the channel. Using IR Fourier spectroscopy and X-ray photoelectron spectroscopy (FTIR and XPS), the authors show that the main reason for this is oxidation, since EDT does not completely protect the NC surface. In the study of charge mobility in PbSe NC films 6 nm in diameter [8], it was shown that the measurement of the current strength is possible for a period of less than 500 ms, until screening charges have time to accumulate from the channel . We have recently shown that a similar effect is observed in thin films of PbS nanocrystals with an EDT ligand shell [3].

Another reason for charge accumulation is the formation of trap states on the surface of the dielectric (for example, acceptor states in silicon oxide) and at the interface between the dielectric and the active layer [9]. In this connection, the choice of dielectric plays an important role. And while in the case of a conventional bottom-gate transistor with an insulating layer of silicon oxide and pre-applied metal electrodes, dielectric replacement is not possible and only surface modification is available using surface treatment with silanes, in other cases, partial or complete replacement of the layer material is possible . These include schemes where metal electrodes are deposited after an additional polymer layer is deposited on the oxide surface of the substrate [10,11], as well as transistors made according to the top-gate scheme using a polymer insulator. In the latter case, it should be taken into account that the choice of polymer has a great influence on the results. For example, Ref. [12] describes the differences in the operation of the top-gate transistor when using different polymer insulators (Cytop fluoroplastic, PMMA polymethyl methacrylate and PVDF polyvinylidene fluoride), due to different permittivity and different ability to form trapping states.

The problem of the influence of trap states on the measurement results is also known from a comparative analysis of mobility measurements by the field-effect transistor method and from measurements of space-charge limited current (SCLC) [13]. For example, it was shown that a high density of traps in PbS NC layers prevents band-like transport of charge carriers at low bias. In the case of using $CsPbBr_3$ perovskites, an additional factor affecting the measurement results is the effect of ion migration — a high concentration of ions leads to screening of the gate field [14]. To overcome ion migration, a reasonably high voltage is required, which not only makes it difficult to determine mobility, but also imposes restrictions on the operation of field-effect transistors and devices based on them, such as LEDs and photodetectors.

2. Materials and methods

A commercial *n*-channel IRF640N field-effect transistor was used as a reference sample. Zinc oxide (ZnO) nanoparticles, fullerene derivative PCBM ([6,6]-phenyl-C_{61}-butyric acid methyl ester) and conductive polymers PEDOT:PSS (poly(3,4-ethylenedioxythiophene) polystyrene sulfonate) and PTB7 (Poly[[4,8-bis17(2-ethylhexyl)oxy]benzo[1,2-b:4,5-b′]dithio-phene-2,6-diyl][3-fluoro-2-[(2-ethylhexyl)carbonyl]thieno[3,4-b]thiophenediyl]) were purchased from Sigma-Aldrich (Merck). PbS nanocrystals were synthesized by hot injection [15]. Long chain ligands of oleic acid were removed, and the NC surface was passivated with lead iodide (PbI_2). Thin films (50−70 nm) of these materials were obtained by spin-coating from a solution onto a rotating substrate. The substrates were preliminarily cleaned with organic solvents in an ultrasonic bath, with subsequent plasma cleaning. Polycrystalline $MAPbI_3$ films (300 nm thick) were obtained by antisolvent crystallization followed by thermal annealing [16]. Volt-ampere curves were obtained using a Keithley 2636b picoammeter.

The silicon substrates used in this work (Ossila Prefabricated OFET Test Chips, Low-Density) for transistors with the bottom-gate structure, as well as the silanization procedure with hexamethyldisilazane (HMDS) are described in [3]. To fabricate the top-gate structure, we used an Ossila glass substrate with pre-applied ITO electrodes (ITO Glass Substrates, 20×15 mm, OFET and Sensing). After the sample deposition on the substrate, a PMMA film with a thickness of about 400 nm was applied to it (also by applying a 60 mg/ml solution of PMMA in toluene to a rotating substrate), after which a silver electrode with a thickness of 100 nm was applied by thermal vacuum deposition through a mask.

All calculations were carried out according to the formula for the linear mode, while the drain curves did not show saturation.

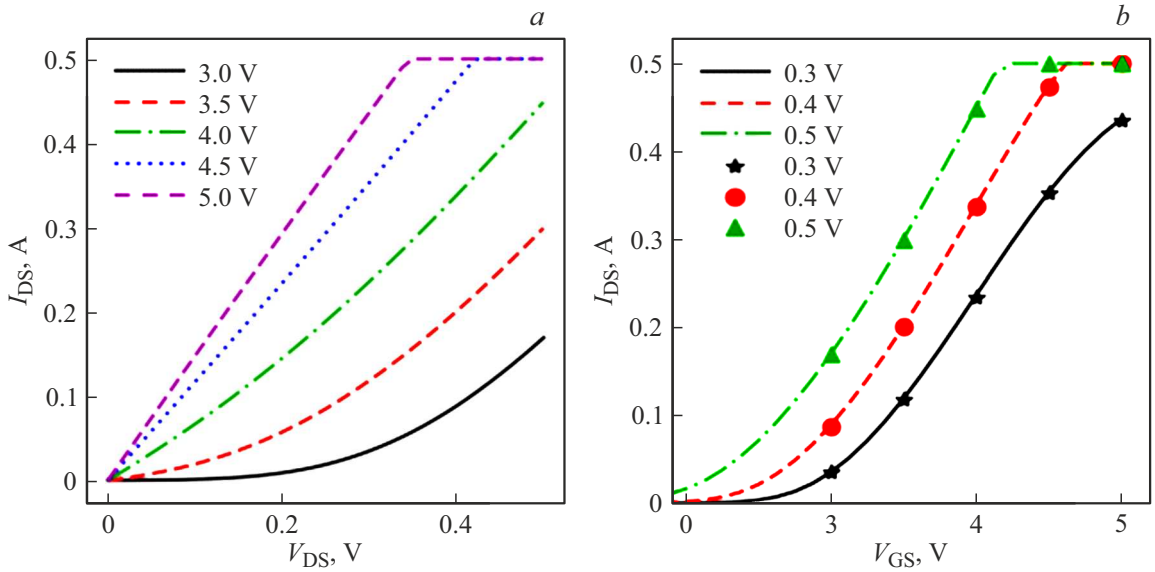

Figure 1. Field effect transistor IRF640N. *a* — drain characteristics (hereinafter, the fragment *a* shows the gate voltage), *b* — drain-gate characteristics (lines show the experimental data, symbols correspond to the recalculated data, hereinafter, the fragment *b* indicates the drain voltage).

3. Test samples

To begin with, we checked whether the data differ when examining a silicon field-effect transistor. As discussed above, the value of mobility can be obtained from a slope analysis of the drain-gate characteristic, the latter also being obtained from a series of drain characteristics taken at a constant value of the gate voltage. Theoretically, these data should match, since the drain characteristics can be put in correspondence with the drain-gate ones, and vice versa. In the case of a commercial *N*-channel field-effect transistor IRF640N, all the data coincide and the points from the recalculated drain curves exactly fit the experimental data (Fig. 1). The mobility calculation was not carried out, since the geometric dimensions of the transistor channel and its capacitance are not given in the documentation.

Next, we investigated commercially available materials — ZnO nanocrystals (with electron-type conductivity) and conductive PEDOT:PSS polymer (with p-type conductivity). In the case of PEDOT:PSS, the hole mobility calculated from the linear part of the drain-gate characteristic in the range from -8 to -2 V was $3.7 \cdot 10^{-2}$ cm^2/(V · s) (Fig. 2, *b*).

The mobility value based on the calculation from the drain curves (Fig. 2, *a*), corresponding to the voltage -5 V, was $5.8 \cdot 10^{-2}$ cm^2/(V · s), which is 1.6 times greater than the experimental value.

The linear part of the drain characteristic of the film of ZnO nanocrystals begins with a shift of 10 V (Fig. 3, *a*), probably due to the barrier formed on the contacts. It can be seen in the drain-gate characteristic (Fig. 3, b) that at a drain voltage of 10 V, the turn-on voltage exceeds 20 V and it is difficult to determine the slope of the curve, but at a drain voltage of 20 V, the dependence is linear, and the mobility is $4.6 \cdot 10^{-6}$ cm^2/(V · s). The drain-gate curves were recalculated from the drain curves approximated by a linear function over the interval 10–40 V. The slope of the recalculated characteristic corresponding to 20 V is slightly less than the experimental one, and it corresponds to the mobility $4.2 \cdot 10^{-6}$ cm^2/(V · s).

Comparison of the results obtained for two high-resistance samples (PEDOT:PSS, ZnO) and a reference commercial transistor shows that for materials that are more difficult to measure, the slope of the recalculated drain-gate curve can be approximately 20% higher than the experimental one.

4. $MAPbI_3$ film

The deviation shown above is characteristic not only of materials with poor conductivity, but also of materials that are characterized by hopping conductivity and trap states (polycrystalline and amorphous semiconductors). As such an example, we considered a $MAPbI_3$ perovskite film, which is a polycrystalline structure.

The drain and drain-gate characteristics of a $MAPbI_3$ perovskite film are shown in Fig. 4, and while the drain shows that both types of conduction are manifested, the drain-gate characteristic could be obtained only for *n*-conductivity at a gate voltage of 20 V. The mobility for the segment approximated on the interval from -4 to 5 V was $4.1 \cdot 10^{-6}$ cm^2/(V · s).

Recalculation from stock curves at a voltage of 25 V gave a mobility of $1.3 \cdot 10^{-5}$ and $1.6 \cdot 10^{-5}$ cm^2/(V · s) for *p*- and *n*-channel mode. In this case, it can be seen that the recalculation makes it possible not only to see the

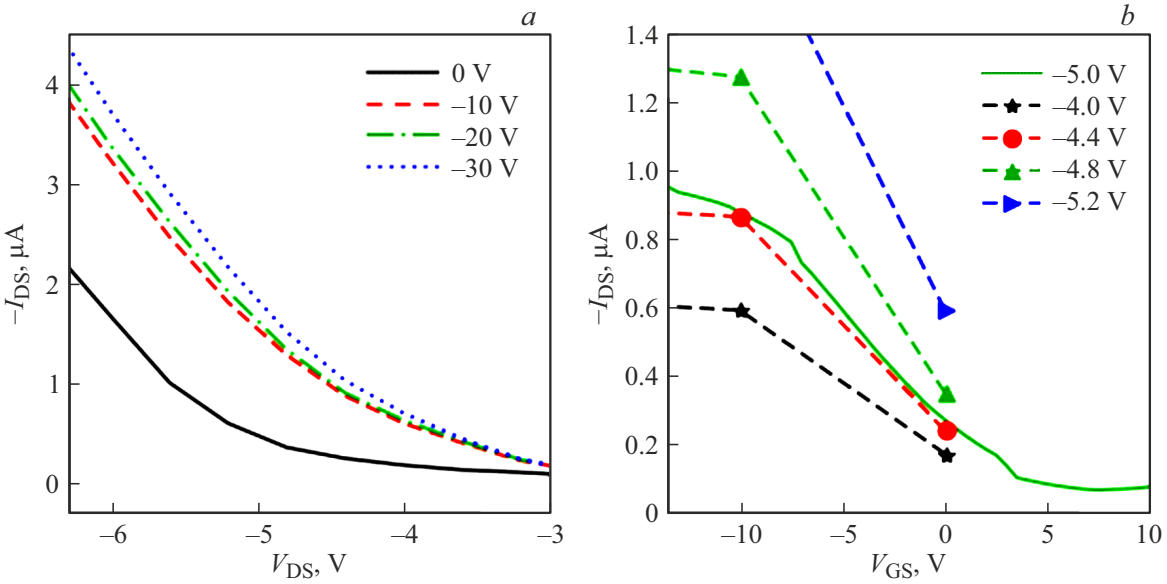

Figure 2. PEDOT:PSS film. *a* — drain characteristics obtained at gate voltage V_{GS} from 0 to −30 V; *b* — drain-gate characteristics (solid line — experimental data, obtained at $V_{DS} = 5$ V, symbols connected by dashed lines — recalculated for the indicated values of V_{DS}).

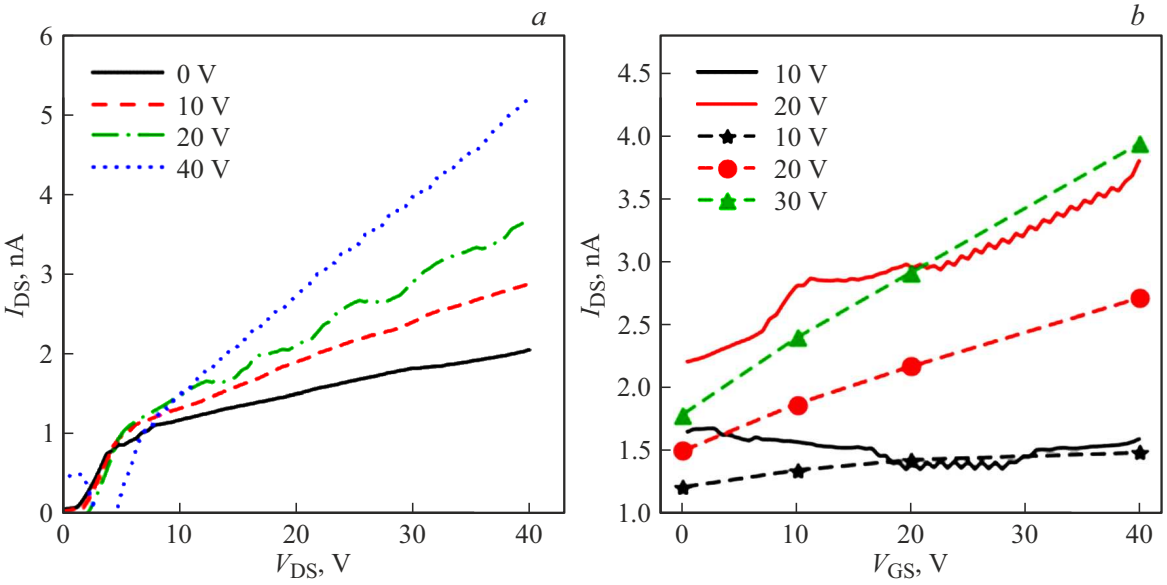

Figure 3. ZnO NC film. *a* — drain characteristics, *b* — drain-gate characteristics (solid lines — experimental data, symbols connected by dashed lines — recalculated data).

underestimation of values, but also to obtain data when the usual method of measurement does not give a result.

5. PbI–PTB7–PCBM

NC-based devices often additionally use conductive additives that improve charge transport. Therefore, we studied a sample of a film deposited from a colloidal solution of PbS nanocrystals with the addition of a conductive polymer with hole conductivity PTB7 and fullerene PCBM providing electronic conductivity (in the proportion of 9 : 1 : 1).

The plot of the drain-gate characteristics shows that the slope of the experimental and calculated curves differs at low voltage and practically coincides at high voltage (Fig. 5). The calculation of the mobility from the drain-gate curve at −5 V shows some underestimation of the experimental data relative to the recalculated data — $6.5 \cdot 10^{-4}$ versus $8.2 \cdot 10^{-4}$ cm^2/(V · s). However, there are no problems with measurements caused by the accumulation of charge, as in the case without the use of a conductive polymer.

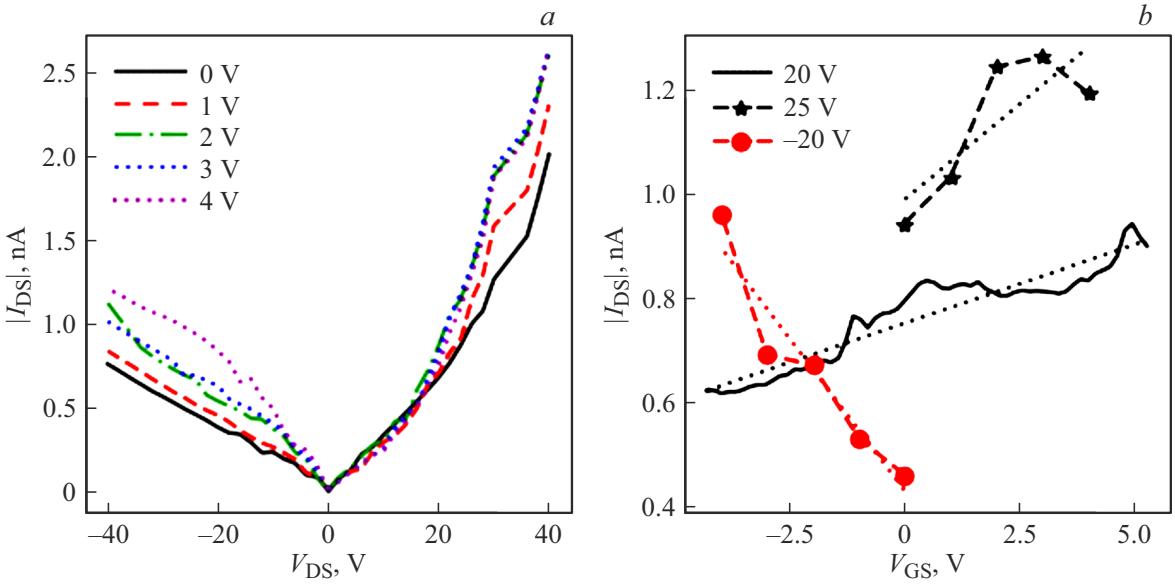

Figure 4. Perovskite film $MAPbI_3$. *a* — drain characteristics (gate voltage is indicated by its absolute value), *b* — drain-gate characteristics (solid line — experimental, dashed lines – - recalculated data, dotted line — approximation by linear functions).

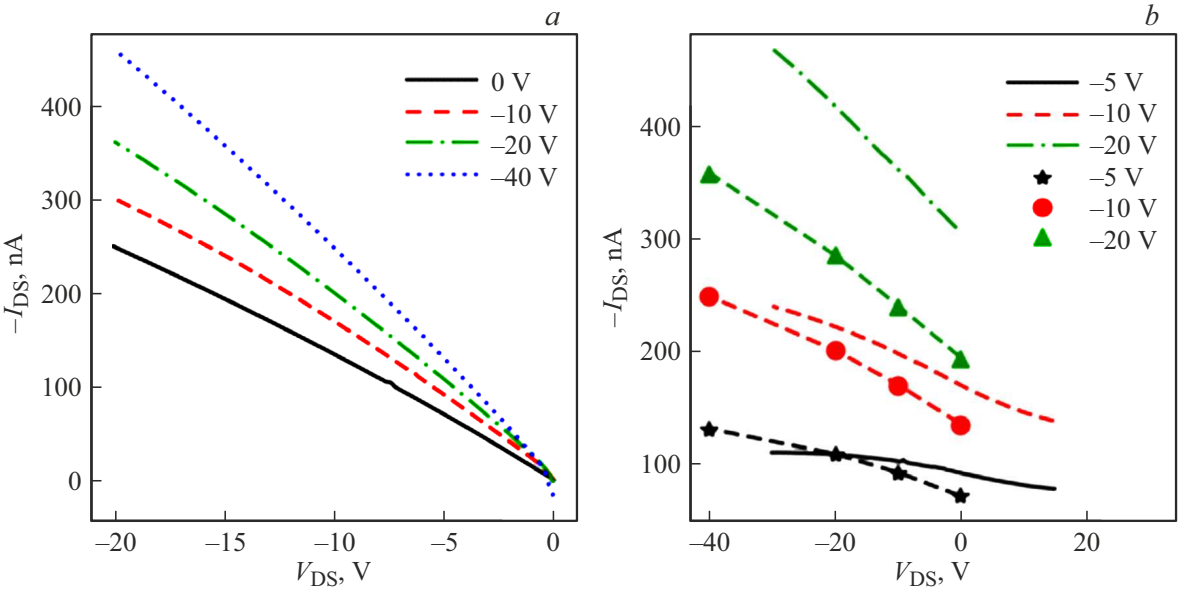

Figure 5. PbI–PTB7–PCBM film on silicon substrate, bottom-gate structure. *a* — drain characteristics, *b* — drain-gate characteristics (lines — experimental data, symbols connected by dashed lines — recalculated data).

For comparison, we examined the same film in the top-gate structure with PMMA as an insulator, which is often used in such structures. As before, only hole conduction is visible (Fig. 6). Unlike the previous case, with the bottom-gate structure, the currents and voltages are smaller, and the mobility data obtained at -5 V differ more — $1.2 \cdot 10^{-4}$ and $2.4 \cdot 10^{-4}$ $cm^2/(V \cdot s)$ for the experimental and recalculated curves, respectively. This shows that the effect under consideration is explained not only by the channel material itself, but also by its interaction with the insulator.

6. Results and discussion

The results are summarized in a table; literature data on similar samples are also given. The $MAPbI_3$ perovskite mobility value is in a wide range and is determined by the technology of layer fabrication. The values for the PbI–PCBM–PTB7 composite are given for all three components, and the measured value correlates with the composition.

In most cases, the data obtained using the recalculated drain characteristics look overestimated relative to the data

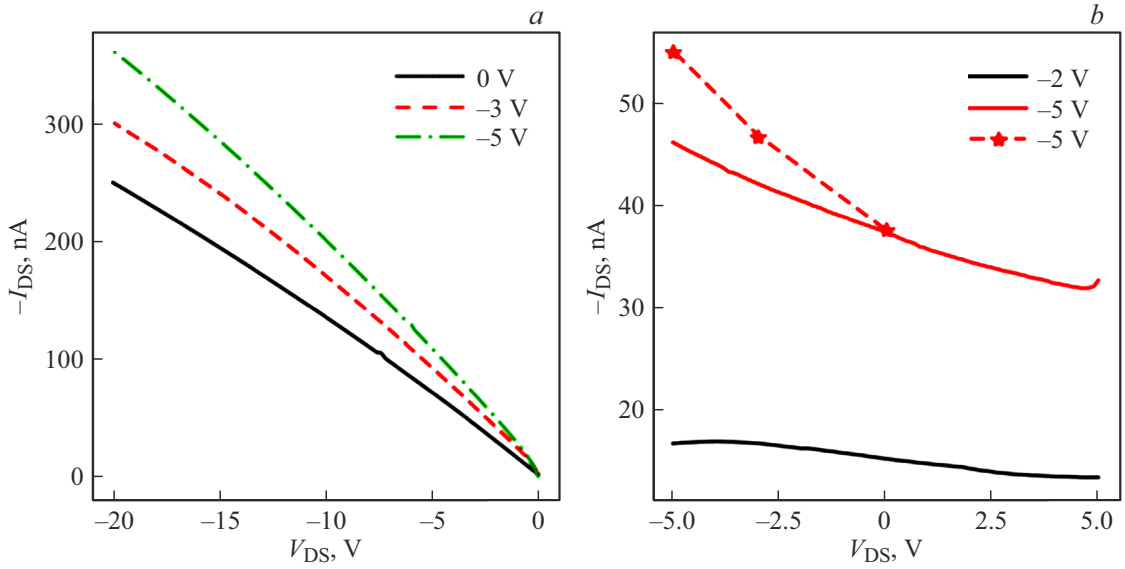

Figure 6. PbI–PTB7–PCBM film on a glass substrate, top-gate structure. *a* — drain characteristics, *b* — drain-gate characteristics (solid lines — experimental data, symbols connected by a dashed line — recalculated data).

Comparison of methods for calculating charge mobility

Sample	Experimental values $cm^2/(V \cdot s)$	Comparison	Recalculated values $cm^2/(V \cdot s)$	Literature data, $cm^2/(V \cdot s)$
IRF640N, μ_e	–	=	–	
PEDOT:PSS, μ_h	$3.7 \cdot 10^{-2}$	<	$5.8 \cdot 10^{-2}$	10^{-1}–10^{-2} [17–18]
HK ZnO, μ_e	$4.6 \cdot 10^{-6}$	~	$4.2 \cdot 10^{-6}$	10^{-6}–10^{-4} [19–20]
$MAPbI_3$, μ_h	–	–	$1.3 \cdot 10^{-5}$	$5 \cdot 10^{-6}$–50 [21–22]
$MAPbI_3$, μ_h	$4.1 \cdot 10^{-6}$	<	$1.6 \cdot 10^{-5}$	See above
PbI–PTB7–PCBM („bottom-gate“), μ_h	$6.5 \cdot 10^{-4}$	<	$8.2 \cdot 10^{-4}$	PCBM: 10^{-3}–10^{-2} [23–24] PTB7: $5 \cdot 10^{-5}$–$3 \cdot 10^{-4}$ [24] PbS: $2 \cdot 10^{-7}$–$2 \cdot 10^{-3}$ [3]
PbI–PTB7–PCBM („top-gate“), μ_h	$1.2 \cdot 10^{-4}$	<	$2.4 \cdot 10^{-4}$	See above

obtained in the classical way from the drain-gate curves. We believe that the data obtained from the drain curves are generally more reliable, since there is no continuous charge accumulation, which additionally affects the current in the channel, and the method allows obtaining data where they could not be obtained from the drain-gate curves. Therefore, we believe that in the considered cases, the discrepancy indicates an underestimation of the data obtained from the drain-gate curves, rather than an overestimation of the data obtained from the drain characteristics.

As such, the discrepancy between the data obtained by the two methods indicates that the trap states and charges at the interface between the media under study and the insulator significantly affect the process of charge carrier transfer in the studied layer (which can be differentiated in individual experiments, for example, with insulator modification).

The main disadvantage of the method for calculating mobility from drain curves is that instead of obtaining a single drain-gate curve, a series of drain curves is required, which is associated with an increase in measurement time, especially for obtaining data of comparable quality. So, if the drain-gate curve consists of N points, then a similar number of drain curves is required to obtain comparable data. In some cases, especially when measuring organic and perovskite materials, under the influence of current during the measurement time, the properties of the material under study can change noticeably. Therefore, a trade-off between data quality and measurement time may be required.

Conclusions

The mobility of charge carriers in materials with low conductivity, as well as in films of nanocrystals, was

measured based on the calculations using the drain and drain-gate characteristics of a field-effect transistor. It is shown that it is better to calculate the mobility of such materials based on drain characteristics, since the common use of drain-gate characteristics can lead to a systematic error caused by charge accumulation in the transistor structure.

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Conflict of interest

The authors declare that they have no conflict of interest.

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