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Study of InP/GaP quantum wells grown by vapor phase epitaxy

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We consider structure with single quantum well InP 5 nm thick grown by vapor phase epitaxy on n-GaP wafer. By classical capacitance-voltage profiling of Schottky diode on sample and electrochemical profiling, electron accumulation were detected in InP layer so existence of quantum well is confirmed. Results of admittance spectroscopy and deep-level transient spectroscopy showed defect formation in GaP layers above InP with energy position of Ec-0.21 eV, 0.30 eV and 0.93 eV.

Keywords: quantum well, capacitance-voltage profiling, electrochemical profiling.

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The fabrication of optoelectronic heterostructures based on A^3B^5 semiconductors on silicon substrates is currently a actual problem. One priority area for photovoltaics is the production of adouble-junction solar cell on a silicon substrate: the lower subcell is based on an A^3B^5/Si heterojunction with the space-charge region (SCR), where the process of carrier separation on absorption of radiation is the most efficient, embedded into silicon with bandgap width $E_g = 1.12$ eV, and the upper subcell is based on A^3B^5 photoactive materials with $E_g = 1.7-1.8$ eV. Solid solutions of GaP with nitrogen (GaPN ternary compounds [1], quantum-dimensional GaP(N)/InP structures featuring a large number of alternating GaP(N) and InP layers with their thickness ranging from a single monolayer to 10 nm [2], and (In)GaPN(As) quaternary compounds [3]) may be used as a base for such materials. However, it has already been demonstrated that non-radiative recombination centers form in greater numbers in semiconductor layers of this kind due to the incorporation of nitrogen into the phosphorus sublattice in GaP, thus shortening the lifetime of minority carriers and reducing the efficiency of photoconversion structures. That said, the method of alternating quantum-dimensional layers has been applied successfully in InAs/GaAsN heterostructures for solar cells [4] grown by molecular beam epitaxy on GaAs substrates, and Si/GaP superlattices [5] have been produced by atomic-layer plasma-chemical deposition. Thus, the fabrication of short-period InP/GaP and InP/GaN superlattices may be of interest for photovoltaics applications. The possibility of fabrication of periodic InP/GaP structures of this kind on GaAs substrates [5,6] with the bandgap width varying from 1.65 to 2 eV depending on the number of periods and the layer thickness has been demonstrated earlier. However, the fabrication of InP/GaP quantum wells (QWs) on silicon substrates is currently a relevant topic and still presents a serious challenge [7–9].

The growth of periodic heterostructures on silicon and gallium phosphide substrates is advantageous in photovoltaics due to the similarity of lattice constants; this is the reason why the present study is aimed at examining the possibility of fabrication of a single InP QW on GaP substrates by vapor phase epitaxy and analyzing the process of defect formation in such structures with the use of capacitance techniques.

Epitaxial *n*-type GaP layers were grown by metalorganic vapor phase epitaxy using an Aixtron AIX200 setup with a horizontal reactor under a reduced pressure (100 mbar) and temperatures varying from 600 to 700°C. Trimethylgallium ($Ga(CH_3)_3$) and trimethylindium ($In(CH_3)_3$) were used as sources of group III elements, and phosphine (PH_3) was the source of phosphorus (group V element). Silane (SiH_4) served as the source of silicon (*n*-type dopant impurity). Layers of *n*-GaP with a single InP/GaP QW were grown sequentially on an *n*-GaP substrate with electron concentration $n = (1-2) \cdot 10^{18}$ cm^{-3}. The studied structure is presented in the inset of Fig. 1. An Ohmic contact to the back side of the *n*-GaP substrate was formed by depositing an indium layer; in order to minimize the contact resistance, contacts were annealed at a temperature of 450°C in nitrogen for 1 min using a JIPelec JetFirst100 system. In order to perform capacitance measurements, gold, which was needed to form a Schottky barrier to *n*-GaP, was deposited onto the face side of the structure by thermal sputtering through a mask with apertures 1 mm in diameter. The resulting current-voltage curve of the sample corresponded to the one of a Schottky diode: the current density under reverse bias was low, and exponential behavior was observed under forward bias (Fig. 1).

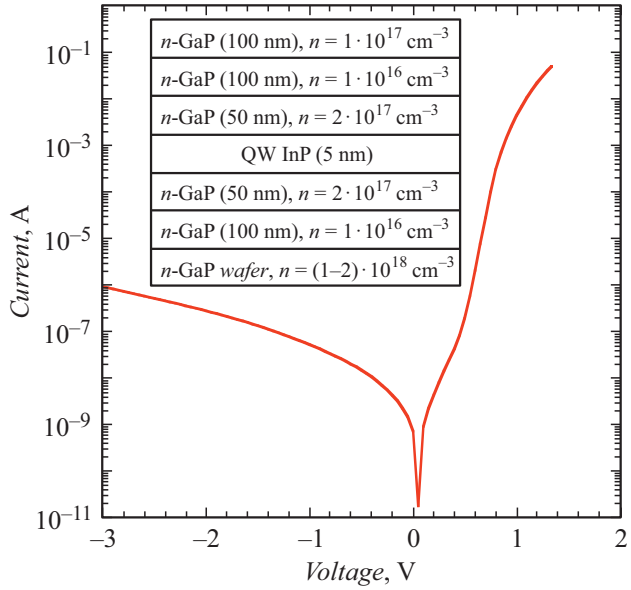

Figure 1. Current–voltage curve with a formed Schottky barrier. The schematic diagram of the structure is shown in the inset.

Measurements of capacitance-voltage curves (C-V) and DLTS (deep-level transient spectroscopy) spectra for the obtained Schottky diodes were performed using a Boonton-7200B capacitance meter at a frequency of 1 MHz, and admittance spectroscopy was carried out with an LCR Agilent E4980A-001 precision meter in a Janis CCS-400H/204 closed-cycle helium cryostat within the temperature interval of 12–800 K. Figure 2 presents the C-V measured at different temperatures (a) and the profiles of concentration $N_{cv}-W$ of free carriers calculated based on these C-V (b). All profiles feature peaks at a depth of approximately 320 nm. This confirms the presence of a narrow nanoscale layer with the electron concentration raised due to the presence of an InP QW. In addition, it follows from experimental data that profiling of the upper GaP layers is observed at temperatures above 400 K, but cannot be achieved at lower temperatures (100−300 K) due to a reduction in the concentration of majority carriers and the corresponding expansion of the space charge region [10].

The distribution profile of the electron concentration in the initial structure was studied next by electrochemical profiling with the use of an ECVPro (Nanometrics) profilometer and LCR Agilent E4980A-001 in the classical mode of capacitance–voltage profiling (depletion mode) and by controlled etching of the semiconductor material (etching mode). An NH_4HF_2 (0.2 M) solution with an added surfactant (Triton X100) was used as an electrolyte. The test signal amplitude was 100 mV, the frequency was 277 Hz, the operating point was 0.24 V, and the etching current was 0.4−0.6 mA/cm^2. Figure 2, c presents the results of profiling for both modes. The carrier concentration profile in the etching mode correlates with the one obtained above in C-V measurements for the sample with a Schottky barrier: the concentration peak ($1 \cdot 10^{17}$ cm^{-3}) is observed at a depth of 300 nm from the sample surface. An SCR profile with a well-pronounced peak, which corresponds in shape to a QW at a depth of 297 nm with a peak concentration of $9 \cdot 10^{16}$ cm^{-3} (the electron concentration in the substrate is $2.5 \cdot 10^{18}$ cm^{-3}), was also obtained in the depletion mode.

Thus, the experimental data suggest that an InP/GaP QW may be formed on a GaP substrate. It is also of interest to study the influence of a well on the process of defect formation in surrounding GaP barrier layers. Capacitance DLTS and admittance spectroscopy measurements were carried out for this purpose. According to the C-V, profiling of the well itself and subjacent GaP layers (through to the substrate) occurs at 300 K (Fig. 2, a) as the reverse bias increases. In contrast, band flattening is observed when forward bias is applied, the measured capacitance increases sharply, and the calculated concentration profile is indicative of penetration of the space charge region into GaP layers above the well. In addition, the concentration of free carriers increases as the temperature grows from 300 to 600 K; therefore, the space charge region shrinks, and its boundary may penetrate into the well itself and the upper GaP layers in the process of heating. With this behavior of capacitance, the measurement parameters (applied bias voltage and temperature) are of critical importance. Figure 3, a presents the DLTS spectra for different modes of measurement of relaxation of the barrier capacitance: (i) initial bias voltage $V_{init} = 0$ V and filling pulse $V_{pulse} = +2$ V with a duration of 50 ms, which corresponds to scanning of the upper GaP layers; (ii) $V_{init} = -5$ V and $V_{pulse} = +5$ V, which corresponds to scanning of GaP layers below the QW at a frequency of 1 MHz and a temperature lower than 300 K. Three peaks are observed in DLTS spectra measured under forward bias: the first peak is found in the 110−140 K temperature interval and represents defect $E1$ with activation energy $E_a = 0.21$ eV, capture cross section $\sigma = 6 \cdot 10^{-15}$ cm^2, and concentration $N_{E1} = 1.5 \cdot 10^{15}$ cm^{-3}; the second one (150−180 K) corresponds to defect $E2$ with $E_a = 0.30$ eV, $\sigma = 3 \cdot 10^{-15}$ cm^2, and $N_{E2} = 3 \cdot 10^{14}$ cm^{-3}; and the third one (380−450 K) corresponds to defect $E3$ with $E_a = 0.93$ eV, $\sigma = 1 \cdot 10^{-13}$ cm^2, and $N_{E3} = 6 \cdot 10^{15}$ cm^{-3}. Similar sets of peaks are observed under reverse bias, but their amplitudes are lower: the $E1$ and $E2$ response intensity (these peaks are enlarged in the inset of Fig. 3, a) decreases by more than an order of magnitude, while $E3$ becomes three times weaker. It is crucial that, according to the carrier concentration distribution, profiling of the upper GaP layers at 100−300 K does not occur under a reverse bias varying from 0 to −1 V, since they are fully depleted initially. In contrast, the calculated SCR at 410 K is smaller than the thickness of the upper GaP layers at 0 V; therefore, these layers are profiled in the direction of the quantum well as the reverse bias increases to −1 V. This is the difference between low- and high-temperature CVCs that explains why the $E3$ response is detected in both DLTS modes, while the first two levels manifest themselves much more clearly under forward bias.

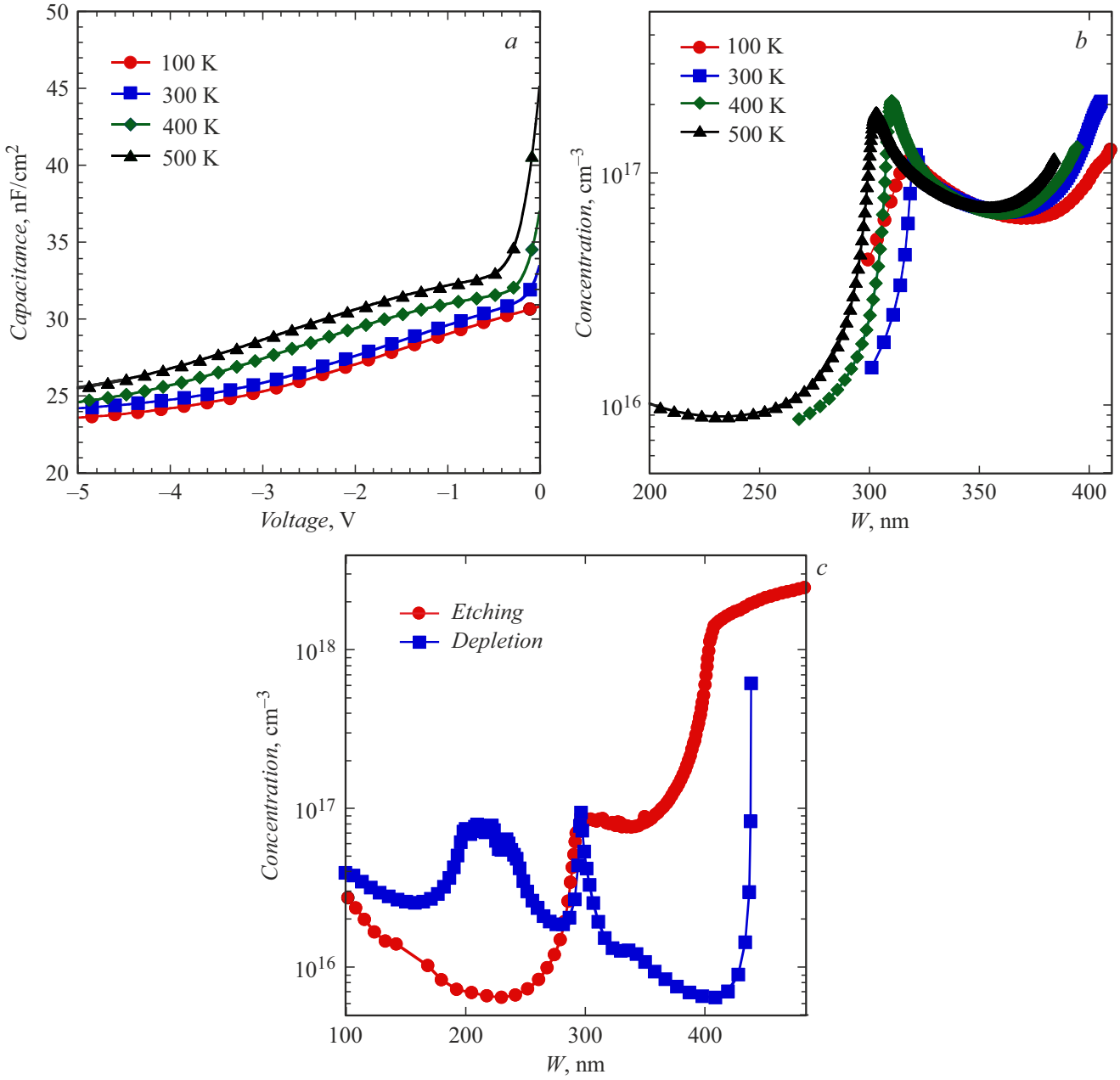

Figure 2. Capacitance-voltage curves (a) and calculated profiles of concentration $N_{cv}-W$ of free carriers at 1 MHz and various temperatures (b). c — Electron concentration profiles determined by electrochemical profiling in etching and depletion modes.

The results of admittance spectroscopy performed at various constant bias values V_{DC} (Fig. 3, b) suggest similar conclusions. First, the capacitance step at 120–160 K in $C-T$ curves measured for different frequencies, which corresponds to the $E1$ defect response, is much taller under forward bias $V_{DC} = +0.5$ V than under $V_{DC} = 0$ (Fig. 3, b). Second, the response at 430–560 K (step in $C-T$ curves) corresponding to the $E3$ defect was detected at all probed values of the bias voltage. The discovered defects have also been detected earlier in GaP:Si layers [11–13] and have the following microscopic structure: $E1 - Si_{Ga} + V_P$, $E2 - V_P + V_{Ga}$, and $E3 - P_{Ga} + V_P + V_{Ga}$. Thus, the presence of an InP QW induces a more intense defect formation in GaP layers grown above it.

The feasibility of formation of a single InP/GaP QW with a thickness of 5 nm on a GaP substrate was demonstrated. The accumulation of electrons in this InP/GaP QW was verified by classical capacitance–voltage profiling of Schottky diodes and electrochemical profiling. Admittance spectroscopy and deep-level transient spectroscopy data revealed that the presence of an InP quantum well induces a more intense defect formation in the upper GaP layers. The measured activation energies of defects are 0.21, 0.30, and 0.93 eV below the bottom of conduction band. A

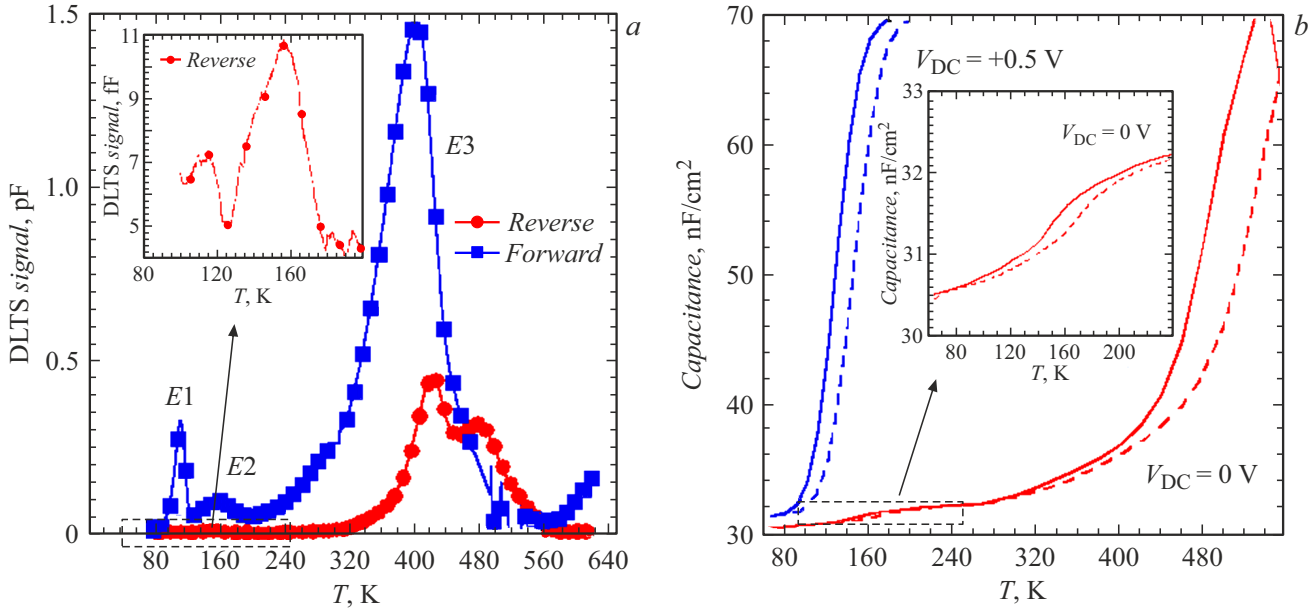

Figure 3. DLTS spectra measured at different V_{init} and V_{pulse} with a rate window of $50\,s^{-1}$ (*a*) and temperature dependences of capacitance at different V_{DC} for 2 kHz (solid curve) and 20 kHz (dashed curve) (*b*).

hypothesis regarding the nature of the discovered defects was formulated.

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Conflict of interest

The authors declare that they have no conflict of interest.

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