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Effect of annealing in an inert atmosphere on the electrical properties of crystalline pentacene films

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The results of a study of the effect of annealing at 150°C in an inert atmosphere $(Ar + 5\% \; H_2)$ on the electrical properties of organic field-effect transistors based on pentacene are presented. Crystalline pentacene films with a thickness of 95 ± 5 nm were obtained using thermal vacuum deposition. The transfer and output characteristics of field-effect transistors before and after annealing for 15 hours are investigated. It was found that as a result of heat treatment, the hole mobility in the saturation regime increased by an average of 30%, and the threshold voltage decreased approximately two times. According to the data of atomic force microscopy, annealing led to a more than twofold decrease in the surface roughness of pentacene films, as well as to a noticeable enlargement of grains, which led to a decrease in the concentration of traps for hole electric transport in the channel of the field-effect transistor.

Keywords: pentacene, vacuum thermal deposition, crystalline films, organic field-effect transistors, hole mobility, annealing in an inert atmosphere.

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For optoelectronics, the preparation of thin crystalline films on substrates of both organic and inorganic semiconductors using vacuum thermal deposition has long been the classical method, distinguished by its simplicity and efficiency [1,2]. At the same time, thin-film crystalline structures obtained in this way, as a rule, are characterized by low structural perfection, since they are polycrystals with grain sizes on the order of hundreds of nanometers. One of the possible ways to improve the morphological quality of the deposited films in order to improve the electrical properties is post-processing under conditions of isothermal annealing at elevated temperature. This approach is very effective for initially amorphous films, in which crystallization is initiated due to subsequent annealing with the formation of large single-crystal regions, which contributes to the significant improvement in electrical properties [1,3]. However, from the point of view of using this approach to improve the structural perfection of crystalline layers of organic semiconductor molecules, which are not prone to the formation of an amorphous phase, there are ambiguous opinions in the literature, which, apparently, is due to the lack of systematic studies. Consider, for example, one of the most well-known and effective organic semiconductors in terms of electrical properties, the pentacene [4,5]. The authors of works [6,7] report that with an increase in the holding temperature in vacuum for 2 h to 70°C, a decrease in the average grain size and a decrease in the surface roughness of pentacene films are observed; at the same time, the mobility of hole transport in the field-effect transistor device increased at exposures up to 45°C, and decreased above this temperature. According to [8], when pentacene thin-film field-effect transistors are held in vacuum for 15 h to 90°C, the increase in the average grain size is observed, and the influence on the hole the mobility is similar: at exposures up to 50°C, there is the almost 2-fold increase, and above this temperature, is decrease to the initial value at room temperature. According to the results [9], exposure to nitrogen flow at temperatures up to 120°C leads to the improvement in the crystalline ordering of molecules in films and the improvement in electrical properties with increasing in hole mobility by almost 4 times in comparison with original unannealed films, and at temperatures from 120 to 240°C, the electrical properties degrade. In the work [10] it is reported, that annealing thin-film field-effect transistors in nitrogen at temperatures up to 180°C reduces the surface roughness of the films and significantly improves their electrical characteristics. On a noticeable improvement in the electrical characteristics of field-effect transistors after annealing for several hours in vacuum at 77°C also reported in the work [11]. There is evidence that when thin-film field-effect transistors are annealed in air for 1 min, the noticeable improvement in electrical characteristics was observed with a maximum for 77°C, and above this temperature, the electrical properties rapidly degraded [12].

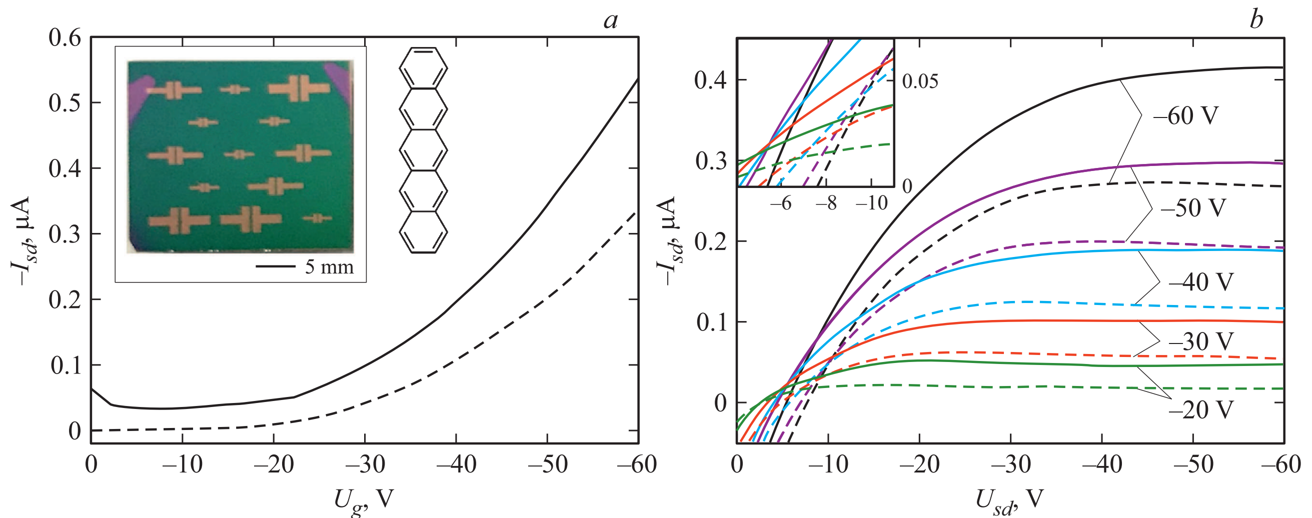

Figure 1. Current-voltage characteristics of the field-effect transistor before processing (dashed curves) and after annealing at 150°C (solid curves). *a* are transfer characteristics at voltage between source and drain $U_{sd} = -60$ V. In the inset, there is a — *p*-Si substrate with organic field-effect transistors (OFET) samples. *b* is the family of output characteristics for different gate voltages U_g. In the inset are dependencies in the linear region.

In order to study the effect of heat treatment on the morphological and structural perfection of deposited thin crystalline films based on semiconductor organic molecules, we initiated systematic studies. In this work, the results of studying the effect of annealing of pentacene (Pc) crystalline films for 15 h at 150°C in an inert atmosphere are presented. It is known from the literature that near 190°C, pentacene exhibits a polymorphic transition to a high-temperature crystalline modification [13], and the processes of sublimation of molecules into the vapor phase [14] are also intensified, which at this stage we would like to exclude from consideration. The study of the electrical properties of pentacene crystalline films, as in the works presented above, was also carried out using the field-effect transistor method [11,12,15,16].

Organic field-effect transistors (OFETs) were fabricated according to the scheme with the lower gate and upper source and drain electrodes [15]. As substrates acting as a gate electrode, silicon wafers 0.5 mm thick doped with a *p*-type impurity (*p*-Si substrates) were used. The role of the gate dielectric on the *p*-Si substrates was played by the SiO_2 oxide layer 440 nm thick, grown by annealing in air at 950°C. The substrates prepared in this manner were etched on one side with concentrated hydrofluoric acid (HF) to remove SiO_2. The substrates were successively cleaned with acetone, isopropanol, and deionized water and kept in the plasma cleaner unit (Harrick Plasma, USA) for 0.5 h during plasma generation from atmospheric oxygen. Next, the film of polymethyl methacrylate (PMMA) from saturated solution in toluene was deposited on the surface of the substrates with the layer of SiO_2 by centrifugation at rotation speed of 3000 rpm on Spin Coater P6700 (Specialty Coating Systems, USA). The thickness of the PMMA buffer layer formed in this way was 30 ± 3 nm. Crystalline films were formed using pentacene (99.9%, Sigma Aldrich) without additional purification. The deposition of Pc, and then the drain and source contacts from gold (99.99%) was carried out by the method of vacuum thermal deposition on COVAP III unit (Angstrom Engineering, Canada), integrated into the SPEKS inert glove box GB 03M (glqq Spectroscopic Systems", Moscow), at chamber pressure $\sim 1 \cdot 10^{-6}$ mbar. The gold contacts were deposited through specially made masks (see the inset in Fig. 1, *a*). The deposition rates of Pc and gold contacts were 0.8 and 0.2 Å/s, respectively. As a result of deposition, the thickness of the pentacene crystalline film was 95 ± 5 nm, and that of the gold contacts was 50 ± 10 nm. In the process of deposition of pentacene films the temperature of the substrates did not exceed 25°C.

The surface morphology of the obtained films was studied using an Ntegra atomic-force microscope (AFM) (NT-MDT, Russia) in the semi-contact method mode (NSG01 series probes with cantilever stiffness 5.1 N/m, resonant frequency 103 kHz, needle curvature radius no more than 10 nm), calibrated according to the TGZ1 sample (NT-MDT). The resulting topograms were processed and analyzed using the Gwyddion [17] program.

The transfer and output current-voltage characteristics (CVC) of OFET devices were studied according to a common-source circuit using a 2612B sourcemeter (Keithley, USA) and Probestation software („Printeltech", Russia) [18] on the LA150DC probe station (Semiprobe, USA) at room temperature. Mobility of charge carriers μ in saturation mode was determined on the basis of the transferring CVCs obtained during the measurement dependences of current values between source and drain I_{sd} on gate voltage

Average electrical characteristics and parameters of the surface morphology of pentacene crystalline films before and after annealing at 150°C (15 h)

Treatment	μ, $10^{-3}\,\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$	U_t, V	R_a, nm	N_a, μm^{-2}
Before annealing	1.9 ± 0.3	-16 ± 2	2.5	45
After annealing	2.5 ± 0.4	-7 ± 3	1.1	25

Note. μ is hole mobility in saturation mode, U_t is threshold voltage, R_a and N_a are average surface roughness and film grain density .

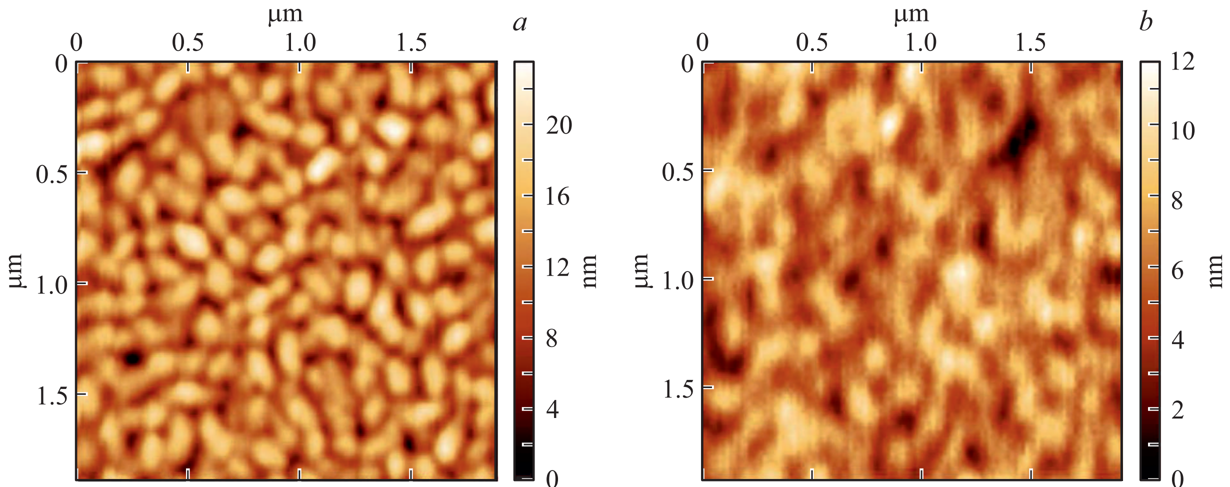

Figure 2. Topographic AFM images of the surface of the pentacene crystalline film before treatment (a) and after annealing at 150°C (b).

U_g using the following expression [11,15]:

$$I_{sd} = \frac{W}{2L}\mu C\left(U_g - U_T\right)^2, \quad (1)$$

where W and L are the width and length of the transistor channel, respectively, $C = 7.3\,\text{nF/cm}^2$ is the specific surface capacitance of the gate dielectric (to estimate C, the permittivity values $\varepsilon_{\text{SiO}_2} = 3.9$, $\varepsilon_{\text{PMMA}} = 3.6$) were used. The channel width W on various samples was 1, 2 and 3 mm, and the channel length L was equal to 100, 200 and 300 μ m respectively, so that the ratio W/L was 10 in all cases.

The samples were annealed for 15 h at 150°C in a flow of a mixture of argon with 5% hydrogen (NII KM, Moscow). Gas flow rate control at the level of 0.3 l/h was maintained using an EL-FLOW Prestige FG-200CV flowmeter controller (Bronkhorst, Netherlands).

The average values of hole mobility μ in the saturation mode and the threshold voltage U_t for a series of 20 field-effect transistors determined before and after annealing are presented in the table. The electrical characteristics of pentacene films established under our conditions before treatment are close to the initial values obtained in the work [11]. As can be seen from the table, isothermal annealing at 150°C for 15 h led to the increase in the average hole mobility by 30% and the decrease in the threshold voltage by about a factor of 2. As an example, Fig. 1 shows the transferring (a) and output (b) CVCs of one of the samples. For this transistor, the mobility has increased by a factor of 1.4 (from $2.1\cdot10^{-3}$ to $2.9\cdot10^{-3}\,\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$), and the absolute value of the threshold voltage decreased from 13.4 to 9.9 V. Estimated from changes in the output characteristics in the linear region (see inset in Fig. 1, b), annealing led to the decrease in the contact barrier at the interface between the Pc film and gold electrodes.

According to AFM data, the thickness of the Pc films changed insignificantly as a result of heat treatment, while the surface morphology and grain structure underwent significant changes (Fig. 2). As can be seen from the topographic AFM images of the surface of the pentacene film shown in Fig. 2, annealing led to a decrease in the average surface roughness R_a by more than 2 fold and coarsening of the grains along with some blurring of grain boundaries (the average density of grains N_a decreased by almost a factor of 2), see the table.

Thus, the improvement in the electrical properties of deposited crystalline pentacene films and the decrease in the contact barrier at the interface with the drain and source electrodes are associated with the structural rearrangement of molecules during annealing in an inert atmosphere. Estimated by the increase in hole mobility μ and decrease in the threshold voltage of field-effect transistors, film annealing reduced the number of traps for electric transport in the transistor channel, which, according to AFM data, is partly due to grain coarsening and an increase in their connectivity (Fig. 2). In the future, it is planned to search for the optimal parameters of thermal-time processing and elucidate the role of the buffer dielectric, the PMMA, in the processes of pentacene recrystallization, leading to a

significant improvement in the electrical characteristics of thin-film field-effect transistors.

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Conflict of interest

The authors declare that they have no conflict of interest.

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