

Influence of chemical treatment and surface topology on the blocking voltage of GaAs thyristor mesastructures, grown by MOCVD

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The effect of sulfide passivation (chemical treatment in a peroxide-sulfur etchant and in a solution of Na₂S in isopropanol) and complication of the profile of the lateral surface of thyristor mesastructures on the blocking ability of GaAs thyristor mesastructures is investigated. It is shown that the blocking voltage of the chips increases several times both after chemical treatment of the surface and with the complication of the surface topology.

Keywords: thyristors, blocking voltage, sulfide passivation, gallium arsenide, mesastructure.

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1. Introduction

Thyristors based on gallium arsenide, grown by Metal-Organic Chemical Vapor Deposition (MOCVD), recently attract attention of researchers in terms of development of low-voltage high-current switches, applied, for instance, for solution of the problem related to generation of short high-peak-current pulses in low-impedance load circuits [1]. Almost all currently known studies on fabrication of A^{III}B^V thyristors (including the ones based on GaAs structures) were performed using high-voltage structures, grown using liquid phase epitaxy method [2,3]. These structures were based on thick (from dozens to hundreds micrometers), lightly-doped ($\sim 10^{14} - 10^{15} \text{ cm}^{-3}$) base layers, providing the switching voltage of $\sim 1 \text{ kV}$. However, these solutions are ineffective, when load has low resistance [1]. The MOCVD method allows to grow thin layers (from tenths to several micrometers) with doping level of $\sim 10^{16} \text{ cm}^{-3}$. In [4,5] the possibility of fabrication of low-voltage thyristors of various design with switching voltage of up to 35 V based on GaAs and its solid solutions using this method was shown. At the same time, the necessity of searching the effective methods for passivation of chip-thyristors side surface was emphasizes, since surface states leaks result in wide spread of samples switching voltage. Since the full process of chip-thyristors manufacturing is rather labor intensive, it is better to study the passivation effects on mesastructures.

One of the main parameters of thyristor as a semiconductor device is a voltage of switching from closed state (with low conductivity) to open (with high conductivity) [6]. However, for thyristor mesastructures it is more correct to use „blocking voltage“ [7] or blockable voltage [8] term, that corresponds to maximum voltage (U_B) in low conductivity state. The further increase of voltage results in sharp increase of current in circuit. It should be noted that contribution to current increase at $U \geq U_B$ can be made by

volume conductivity through thyristor structure by means of avalanche propagation of carriers in strong electrical field of reverse-biased collector $p-n$ -junction or by conductivity related to leaks, that are significantly caused by high density of surface states along the perimeter of $p-n$ -transitions [9]. The contribution from the second component can exceed the contribution from the first one. Therefore, surface breakdown starts at lower values of reverse-biased voltage than in volume.

Chemical treatment with electrolytes solutions allows to efficiently modify the electronic characteristics of A^{III}B^V semiconductor surfaces and interfaces to improve the efficiency of various semiconductor devices based on them [10]. Treatment with sulfide solutions (sulfide passivation) is actively used for electronic and chemical passivation of surface states of gallium arsenide [10,11]. Positive influence of passivation on parameters of device structures based on GaAs and its solid solutions was demonstrated for power diodes [9], lasers [12], photodetectors [13,14], bipolar junction transistors and field-effect transistors [15]. At the same time, it is noted that the same passivation method can result in radically different results for devices of various design, even formed from the same materials [10]. Therefore, the optimum passivation conditions should be selected for each individual structure.

Significant reason for reduction of blocking capability of multi-layer semiconductor devices, diodes and thyristors (both silicon and A^{III}B^V), is generation of inversion channels in the places of $p-n$ -junctions output to mesas side surface, because these channels strongly increase leak currents [16,17]. In case of bulky Si-thyristors (diameter of several centimeters) the electrical field of $p-n$ -junction on a side surface is reduced by means of mechanical profiling (bevels making) for blocking voltage increase [18,19]. At the same time, it is noted that for small-size chips with diameter of several millimeters it is economically reasonable to perform the group treatment using etching methods.

This work is dedicated to studying the possibility of increase of blocking voltage of low-voltage GaAs thyristor mesastructures by means of chemical treatment of their side surface in a peroxide-sulfur etchant and in Na_2S solution in isopropyl alcohol ($i\text{-C}_3\text{H}_7\text{OH}$), and by means of creation of complex-profile stepped topology of mesa side surface using liquid etching method.

2. Investigated samples and experimental method

Thyristor structures were grown by MOCVD $n^+\text{-GaAs}$ (100) substrates with thickness of $450\text{ }\mu\text{m}$ and presented four-layer $n\text{-p-n-p}$ -structure of gallium arsenide layers, doped with silicon (n -type) and carbon (p -type). Emitter layers with thickness of $0.3\text{ }\mu\text{m}$ were doped to concentration of $2 \cdot 10^{17}\text{ cm}^{-3}$. Base region of p -type had thickness of $2\text{ }\mu\text{m}$, charge carriers concentration — $3.5 \cdot 10^{16}\text{ cm}^{-3}$. In the second base with thickness of $1.9\text{ }\mu\text{m}$ the carriers concentration was reduced to $2 \cdot 10^{16}\text{ cm}^{-3}$.

Two types of samples were fabricated using photolithography and chemical etching in solution $\text{H}_3\text{PO}_4 : \text{H}_2\text{O}_2 : \text{H}_2\text{O} = 1 : 1 : 5$ from the plate with grown structure: 1) with simple round mesastructure (first type) and 2) with round mesa with complex stepped profile (second type). Single mesas of the first type with diameter of $d \approx 2\text{ mm}$ were etched to n -base (etching depth $h = 0.6\text{ }\mu\text{m}$) or to substrate ($h = 5.5\text{ }\mu\text{m}$). Second type samples were fabricated using serial etching of three coaxial mesas (Fig. 1): first mesa had depth $h_1 = 5.5\text{ }\mu\text{m}$ and diameter $d_1 = 4\text{ mm}$; second mesa: $h_2 = 0.7\text{ }\mu\text{m}$, $d_2 = 2.7\text{ mm}$ and third mesa: $h_3 = 0.3\text{ }\mu\text{m}$, $d_3 = 0.8\text{ mm}$. Chips with size of $5 \times 5\text{ mm}$ with single mesastructure (simple or stepped) on each one were cut out of the plates. Point ohmic contact was formed on each chip from the substrate side using method of tin foil electrospark burning-in. Indium contact was used from the structure side.

Two methods of chemical treatment of the fabricated mesastructures surface were used in the study. The first method included samples immersion for 1–2 s to peroxide-sulfur etchant (PSE), consisted of concentrated sulfuric acid, 33% hydrogen peroxide and deionized water $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2 : \text{H}_2\text{O} = 4 : 1 : 15$. Then the samples were washed and dried on air. The second method included the abovementioned pre-treatment in PSE and the following sulfide passivation by samples immersion for 3 min into the saturated solution of Na_2S in $i\text{-C}_3\text{H}_7\text{OH}$ at room temperature with additional lighting with 200 W incandescent lamp. After passivation the chips were also washed and dried on air.

Current-Voltage characteristics of thyristor mesastructures were measured in voltage supply mode before and after chemical treatment.

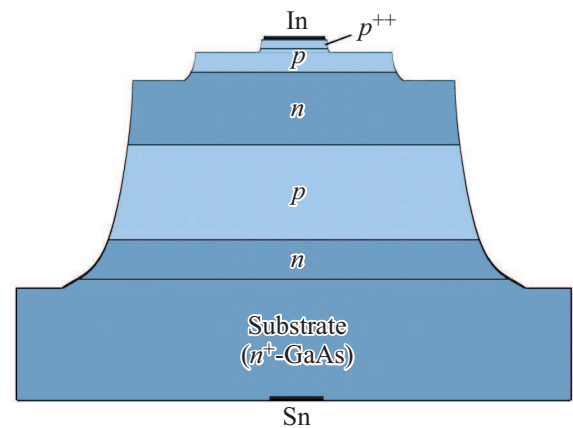


Figure 1. Scheme of the second type sample (chip with stepped mesas).

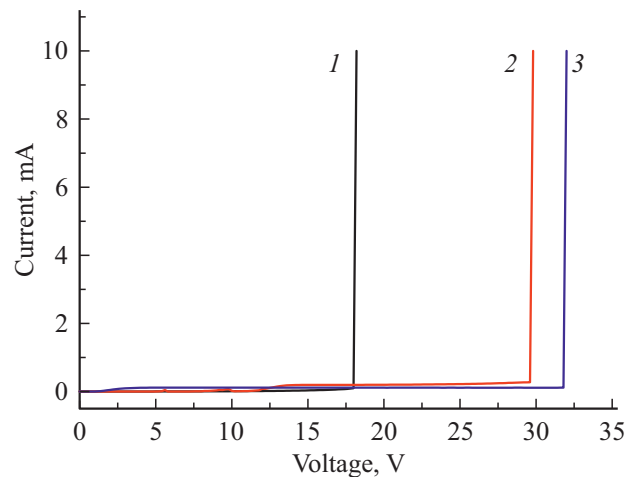


Figure 2. Typical Current-Voltage characteristics (in voltage supply mode) of the first type sample with single mesa with depth of $0.6\text{ }\mu\text{m}$: before treatment (1), after treatment in PSE (2), after treatment in PSE and sulfide passivation in solution of Na_2S (3).

3. Results and discussion

Figure 2 shows typical Current-Voltage characteristics of the first type sample with single mesa with depth of $0.6\text{ }\mu\text{m}$ before and after chemical treatment. It is shown that after samples treatment in peroxide-sulfur etchant the blocking voltage increased from 18 V to $\sim 30\text{ V}$ (Fig. 2, curves 1, 2). Combined treatment of mesastructures surface in PSE and sulfide solution allowed to additionally increase U_B to 32 V (Fig. 2, curve 3). At the same time, the value of reverse current decreased by two orders of magnitude (from 10^{-5} A to 10^{-7} A at reverse voltage $U_R = -20\text{ V}$), that is obviously related to reduction of surface states density at removal of natural oxide and creation of passivating sulfide coating on mesastructures side surface [10,11]. Passivation effect manifestation time at samples storage on air at natural light was $\sim 30\text{ min}$. This is coherent with studies data from review [11], where it was observed that at GaAs surface

exposure in atmosphere and at lighting the passivation effect degraded for 30–40 min by means of natural oxide layer creation. At the same time, the oxidation rate of the passivated surface strongly depended on surface orientation: surface (100) oxidized faster than any other [20]. Therefore, the described above treatment technique can be used, for instance, for quick diagnostics of thyristor characteristics of the grown structure before post-growth plate treatment. In the technology of GaAs thyristors manufacturing it can be used only with additional surface protection (for instance, using protective dielectric coating).

It should be noted that the sharp rise of current through mesastructure at voltage $U \geq U_B$ is often accompanied with breakdown (including surface one) and degradation of thyristor structure. We observed that the blocking capability of chips can be recovered, if natural oxide is removed by etching the thin near-surface layer or when making the new cuts at chips edges. This confirms the surface nature of mesastructure breakdown. Mesas surface treatment, examined in this study, is intended for diminution of degradation effects by means of providing the surface charge, possibly lesser in terms of value and stable in terms of time. The observed results can be used in technology of real devices manufacturing.

Single mesa etching to substrate ($h = 5.5 \mu\text{m}$) on the first type samples significantly reduced the blocking capability of chips. Fast current increase started at voltage $U_B \approx 3\text{--}7\text{ V}$, that can be related to increase of electrical field on the side surface of the deep mesa due to three $p\text{--}n$ -junctions entering this surface (while in case of shallow mesa only one forward-biased $p\text{--}n$ -junction enters this surface).

It is known that liquid etching does not allow to obtain the vertical mesa walls, so they are of concave shape (analogue of straight and reverse bevels). Whether these bevels will make a positive effect (increasing the blocking capability of the structure) or, on the contrary, will make a negative impact, largely depends on the place of entering the side surface of the central blocking junction. Using microscope LEICA DM 4000 M we examined the shape of the side surface of mesas etching. For that purpose we made vertical cuts in the plane, passing through the center of the mesastructure, perpendicular to its layers. It turned out that deep mesa etching creates the straight bevel at the angle of $\sim 45^\circ$ in the area of the central collector $p\text{--}n$ -junction. As per literature it is known that for such angle in silicon thyristors the field intensity on surface is maximum [18], that sharply increase the possibility of surface breakdown. The field intensity significantly reduces on the surface of reverse bevel compared to field intensity in volume at all angles of this bevel. However, it is technically complicated to obtain the reverse bevel on such small objects, therefore the search of ways of protection against surface breakdown continues. When studying the prospects of high-voltage mesa-epitaxial 4H-SiC-diodes protection against edge breakdown by means of creation of mesastructures with sloping walls, forming the straight bevel, the authors [21] concluded that instead of vertical walls it is more efficient to make mesastructures

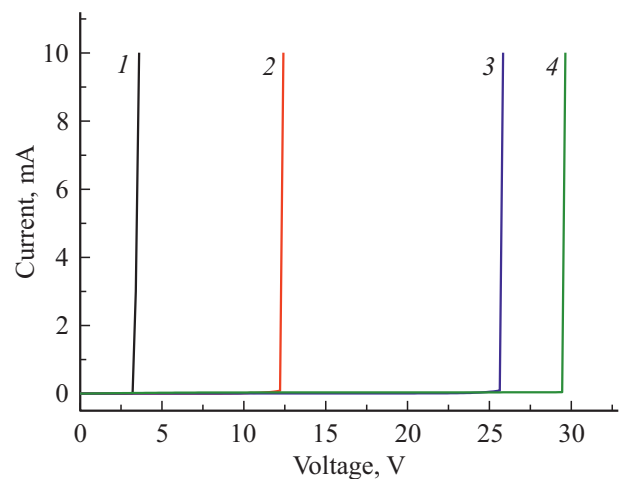


Figure 3. Typical Current-Voltage characteristics (in voltage supply mode) of the second type sample with stepped mesas profile: 1 — one mesa $h_1 = 5.5 \mu\text{m}$; 2 — two mesas: h_1 and $h_2 = 0.7 \mu\text{m}$; 3 — three mesas: h_1 , h_2 and $h_3 = 0.3 \mu\text{m}$; 4 — three mesas and sulphidation.

with sloping walls. As per simulation, when making the straight bevel in 4H-SiC-devices with $p\text{--}n_0$ -junction, there is no need to etch the mesastructure to n -substrate (etching depth is $10 \mu\text{m}$): its etching to the plane of $p\text{--}n_0$ -junction to depth of $1.5\text{--}2 \mu\text{m}$ is sufficient. This corresponds with the results we observed, according to which the maximum blocking voltage corresponds to thyristor mesastructures with single mesa, etched to n -base.

As was mentioned earlier, profiling (bevels creation), reducing the electrical field of $p\text{--}n$ -junction on the structure side surface and, consequently, the surface states leaks, is used to increase the blocking capability of multi-layer semiconductor structures. Based on literature data and our experimental data analysis we developed a three-step geometry of mesas, described in the previous section (second type samples). Depths and diameters of coaxial mesas were selected to decrease the currents of mesas walls surface states leaks, including by means of electrical field intensity reduction in places of $p\text{--}n$ -junctions entering the mesas side surface. After each mesa etching the Current-Voltage characteristics of chips were measured and blocking voltage U_B was registered (Fig. 3, curves 1–3). It turned out that complication of samples surface topology results in increase of U_B value of the structure almost by an order of magnitude (from 3 to 25.5 V). Such change of U_B for structure with complex profile can be related, on the one hand, with removal of heavily-doped contact layer (mesa 3) from the mesa side surface, that complicates the conductivity along surface states. On the other hand, the stepped profile of mesas in some way is similar to bevels with mesa-like contour, proposed for silicon thyristors [22], due to which the surface electrical fields are reduced compared to the fields in materials volume, thus preventing from the structure surface breakdown. As a

result, breakdown of collector transition happens at higher voltage.

Treatment of the developed surface of the second type samples in PSE and alcohol solution of Na_2S allowed to additionally increase the blocking capability to 29 V (Fig. 3, curve 4), that also reflects the reduction of surface states density at the side surface of mesastructures by means of formation of passivating sulfide layer. However, it should be noted, that at repeated measurements of Current-Voltage characteristics the gradual degradation of the blocking capability of the second type chips was observed. Therefore, the additional protection of passivating surface is required.

Comparison of data in Figs. 2 and 3 shows that both methods of mesastructures treatment, used by us, allow to achieve the blocking voltage value of $U_B \sim 30$ V. At the same time, the first method is much simpler in terms of manufacturing technology. However, the results, observed with the second treatment method, can be useful at development of device structures with more complex configuration, for example, thyristors with control electrode.

According to literature, the traditional methods of protection against surface breakdown, well-proven at silicon devices manufacturing (profiling, chemical treatment and side surface protection with dielectric), for gallium-arsenide p - n -junctions are usually insufficient and do not allow to solve this problem completely. Proton and electron irradiation of peripheral areas with energy $E = (3-5)$ MeV and doses of $10^{12}-10^{13} \text{ cm}^{-2}$ [23] were used to extend the range of operating voltage and improve the reliability of GaAs devices. At proton irradiation of n -GaAs its electric conductivity sharply decreases, it becomes high-ohmic and even semi-insulating, that is related to appearance of deep acceptors in the forbidden band of semiconductor. Studies of power pulse diodes, grown using liquid phase epitaxy method, and diodes based on GaAs showed that „low-voltage“ breakdown in non-irradiated structures happened in the area of the boundary mesa-contour of p - n -junction. After proton irradiation the sharp increase of thickness of spatial charge area in peripheral (irradiated) part of the crystal and increase of avalanche breakdown voltage from typical values of 600–800 V to value of > 1000 V were observed. Disadvantage of such treatment is samples radioactivity after irradiation due to initiation of nuclear reactions with high-energy protons.

To strengthen the described effect of increase of the blocking capability of GaAs thyristor mesastructures by means of chemical treatment of their side surface, as well as by means of formation of the developed mesa side surface, the proton irradiation can be performed. Later on we are going to study this topic in detail.

4. Conclusion

Thus, the influence of chemical treatment of the side surface of GaAs thyristor mesastructures, as well as of formation of complex multi-step profile of mesa side surface

on the samples blocking voltage value was studied. The possibility of U_B limit value increase to 30–32 V was shown. This again demonstrates the importance of searching the efficient methods for modification of the electronic properties of surface of gallium arsenide and device structures based on it.

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Conflict of interest

The authors declare that they have no conflict of interest.

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