Comparative study of InP/InGaAs double heterojunction bipolar transistors with InGaAsP pacer at base-collector junction

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In this article, the influence of InGaAsP spacers inserted at base-collector (B-C) junction in the InP/$In_{0.53}Ga_{0.47}As$ double heterojunction bipolar transistors is demonstrated by two-dimensional semiconductor simulation. Due to the addition of an InGaAsP spacer layer, two small potential spikes are formed at B-C junction and the current blocking effect is reduced. The results exhibit that the maximum current gain increases from 30 to 374 (375) as the thickness of InGaAsP spacer layer varies from 0 to 100 Å (300 Å). On the other hand, the device with a thicker spacer layer (300 Å) could effectively improve the knee effect of the current-voltage curves as compared the other devices. In addition, the collector-emitter offset voltages less than 10 mV are observed in the three devices.

1. Introduction

Heterojunction bipolar transistors (HBTs) fabricated by III-V compound semiconductors have attracted significant interest for high-speed digital circuit applications due to their superior performance [1,2]. The large valence band discontinuity (ΔE_V) at base-emitter (B-E) heterojunction could provide a potential barrier for the reverse injection of holes from the base into the emitter to enhance the emitter injection efficiency and current gain. However, the conventional HBTs suffered from a large collector-emitter (C-E) offset voltage (ΔV_{CE}) resulting from the difference of turn-on voltages between B-E and base-collector (B-C) junctions. It will cause large power consumption in circuit applications [3]. To improve the offset voltages, several devices, such as double heterojunction bipolar transistors (DHBTs), heterostructure-emitter bipolar transistors (HEBTs), tunneling-emitter bipolar transistors (TEBTs), etc. have been widely fabricated and demonstrated [4–6].

Furthermore, InP/InGaAs HBTs have been considered to be the promising devices for microwave and optoelectronic integrated circuit (OEIC) applications due to the high electron mobility, high cutoff frequency, and small B-E turn-on voltage [7,8]. Nevertheless, the conventional InP/InGaAs HBT shows a considerably low C-E breakdown voltage resulted from the large electron impact ionization coefficient in the small energy-gap InGaAs collector layer, which is not suitable for power application [8]. In order to reduce the electron impact ionization and increase the breakdown voltage, a large energy-gap InP material is generally employed as a collector layer. Though the traditional InP/InGaAs DHBT could substantially improve the breakdown behavior, the electrons injecting from base to collector will be blocked by the potential barrier due to the conduction band discontinuity ($\delta E_C \approx 0.25$ eV) at InP/InGaAs B-C junction [9]. Thus, the current gain might be severely degraded. Previously, this effect alleviated to reduce the potential barrier at B-C junction by adding an InGaAs spacer and an InGaAs-InGaAsP composite-collector structure had been reported [10]. But, for simplification the single InGaAsP quaternary-compound spacer related to the characteristics of InP/InGaAs DHBTs has not been depicted until now.

In this article, the performance of InP/InGaAs DHBTs with and without the InGaAsP spacer at B-C junction will be comparatively demonstrated. By the use of an InGaAsP spacer layer, the improved transistor characteristics including high collector current, high current gain, and negligent blocking effect will be discussed.

2. Device structures

In the studied InP/InGaAs DHBTs with an InGaAsP spacer layer, the structure layers included a $0.5\,\mu$m $n^+ = 10^{19}\,\mathrm{cm}^{-3}$, $In_{0.53}Ga_{0.47}As$ subcollector layer, a $0.5\,\mu$m $n^- = 2 \cdot 10^{16}\,\mathrm{cm}^{-3}$ InP collector layer, an $In_{0.72}Ga_{0.28}As_{0.61}P_{0.39}$ undoped spacer layer, a $0.1\,\mu$m $p^+ = 10^{19}\,\mathrm{cm}^{-3}$ $In_{0.53}Ga_{0.47}As$ base layer, a 100 Å i-$In_{0.53}Ga_{0.47}As$ layer, a $0.1\,\mu$m $n = 5 \cdot 10^{17}\,\mathrm{cm}^{-3}$ InP emitter layer, and a $0.2\,\mu$m $n^+ = 10^{19}\,\mathrm{cm}^{-3}$ $In_{0.53}Ga_{0.47}As$ cap layer. The devices with 100 Å and 300 Å $In_{0.72}Ga_{0.28}As_{0.61}P_{0.39}$ undoped spacer layers at B-C junction are labeled as devices A and B, respectively. In addition, the third device without the $In_{0.72}Ga_{0.28}As_{0.61}P_{0.39}$ spacer layer, labeled device C, is compared for demonstrating the current blocking effect. All of the three devices, the emitter and collector areas are 50×50 and $100 \times 100\,\mu\mathrm{m}^2$ respectively. A two-dimensional semiconductor simulation package SILVACO was employed to analyze the energy-band diagrams, carrier distributions, and current-voltage (I-V) characteristics [11]. The simulated analysis taked

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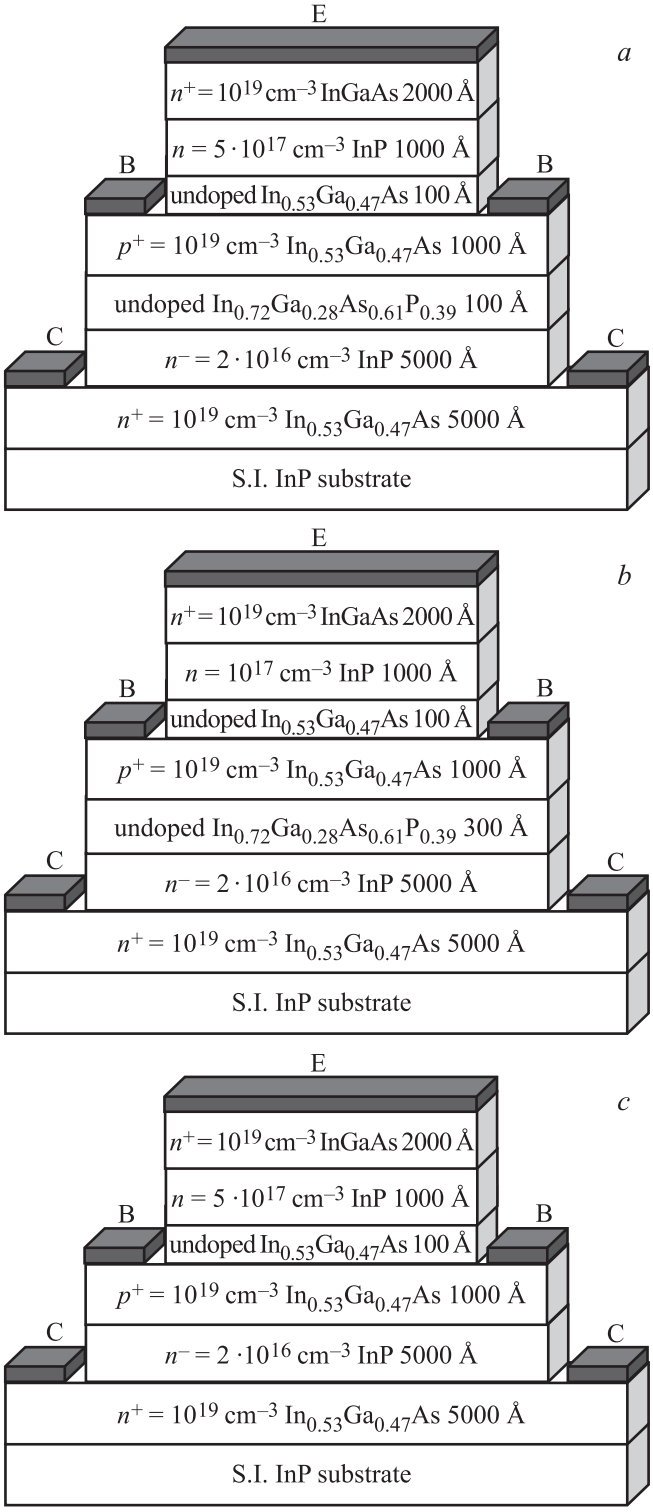

Figure 1. Schematic cross section of (*a*) device A with a 100 Å undoped InGaAsP spacer layer, (*b*) device B with a 300 Å undoped InGaAsP spacer layer, and (*c*) device C without spacer layer at B-C junction.

into account the Poisson equation, continuity equation of electrons and holes, Shockley-Read-Hall (SRH) recombination, Auger recombination, and Boltzmann statistics, simultaneously. Fig. 1 illustrates the schematic cross sections of the devices A, B, and C, respectively.

3. Results and discussion

The energy band diagrams of the devices A, B, and C are shown in Figs 2, *a, b*, and *c*, respectively, at equilibrium and $V_{BC} = -2$ V. In the three devices, the large

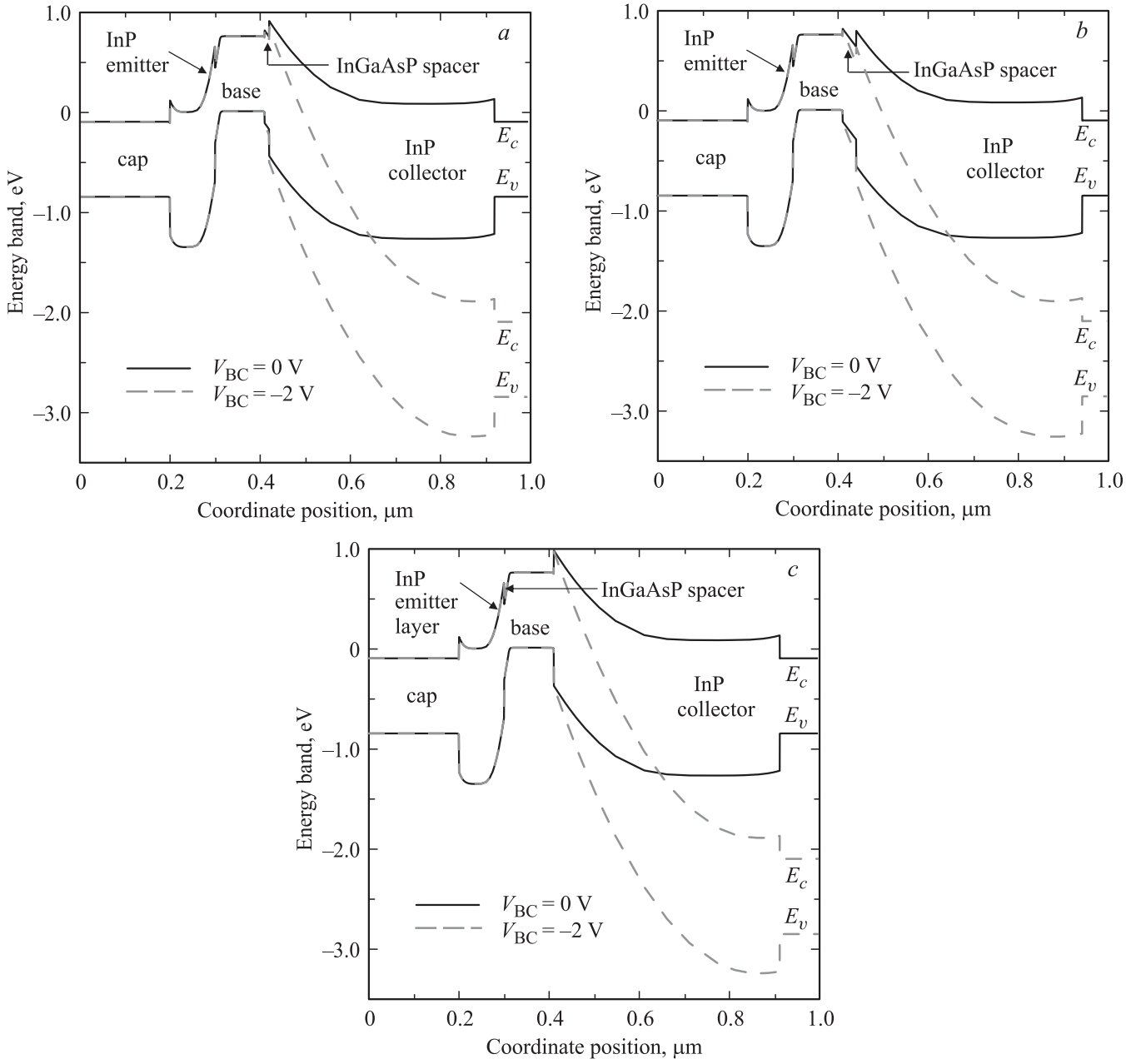

Figure 2. Corresponding energy band diagrams of (*a*) device A, (*b*) device B, and (*c*) device C at equilibrium and $V_{BC} = -2$ V.

valence band discontinuity ($\Delta Ev \approx 0.35$ eV) value at abrupt InP/$In_{0.53}Ga_{0.47}As$ heterointerface near the B-E junction provides relatively good confinement effect for holes to achieve high emitter injection efficiency and current gain [9]. The employment of a thin InGaAs undoped spacer layer between emitter and base layers could help to lower the energy band at emitter side for reducing or eliminating the potential spike at B-E junction. On the other hand, the thin $In_{0.72}Ga_{0.28}As_{0.61}P_{0.39}$ undoped spacer layers are inserted at B-C junction in the devices A and B, which energy gap ($E_g \approx 0.95$ eV) is located between the InP and InGaAs material layers [12]. Obviously, there are two small potential spikes at B-C junction are observed in the devices A and B with the $In_{0.72}Ga_{0.28}As_{0.61}P_{0.39}$ spacers. Also, as compared to the device C, the potential spikes of the device B can be more easily reduced under B-C inverted bias. Nevertheless, a considerably large spike still appeared at abrupt B-C junction in the device C, even at $V_{BC} = -2$ V.

Figs 3, *a, b*, and *c* depict the electronic concentration distributions of the devices A, B, and C, respectively, at thermal equilibrium. Clearly, it can be found that the device B exhibits the highest electron concentration at B-C interface is in because transporting electrons across the B-C junction are easier than the other devices. On the other hand, the device C shows the lowest value, which can be

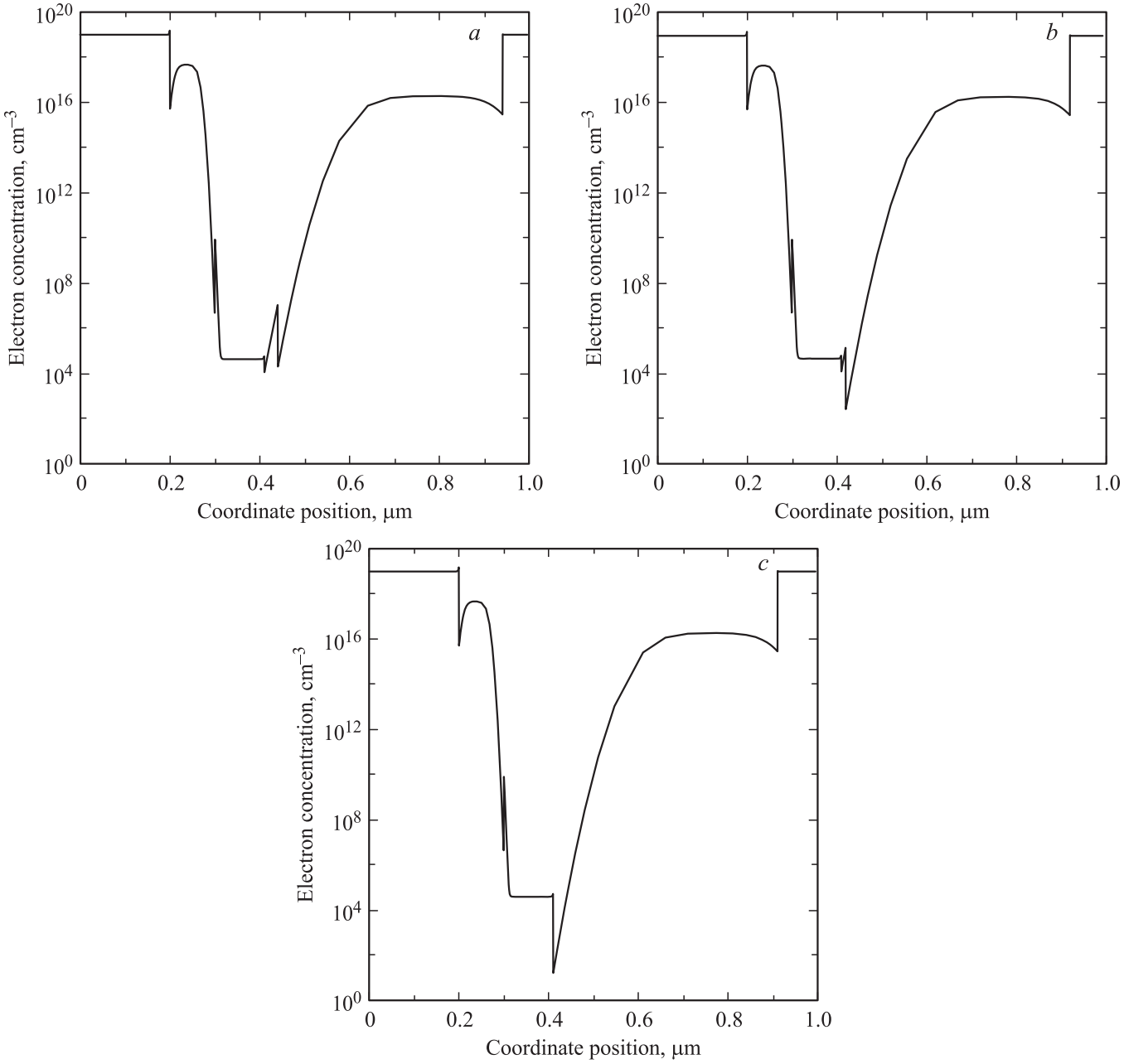

Figure 3. Electron concentration distributions at equilibrium of (*a*) device A, (*b*) device B, and (*c*) device C.

attributed to electron blocking effect by the considerable potential spike at abrupt B-C junction.

The common-emitter current-voltage (I-V) characteristics of the devices A, B, and C are illustrated in Figs 4, *a, b*, and *c*, respectively. The base current IB is applied by 0.1 mA/step. The maximum collector currents are of 148.1, 148.2, and 12.7 mA at $I_B = 0.5$ mA in the devices A, B, and C, respectively. As seen in the I-V characteristics, the maximum current gains of 374, 375, and 30 are obtained in the devices A, B, and C, respectively. That is to say, at sufficiently large C-E voltage (or B-C bias) the blocking of electron transportation is reduced in the devices A and B due to the small spikes, while the transporting electrons across B-C junction are still relatively low in the device C. Furthermore, due to the nearly symmetrical structures of the B-E and B-C junctions, the collector-emitter offset voltages are less than 10 mV in the three devices. It is worthy to note that the insertion of a 300 Å InGaAsP spacer layer can effectively improve the knee effect in the I-V curves. However, the effect still exists in the device A because the InGaAsP spacer thickness is not sufficient to reduce the spike at B-C junction.

Once the B-C terminals are short, i. e., at the boundary of saturation/active operation modes, the simulated Gummel plots of devices A, B, and C are revealed in Figs 5, *a, b*, and *c*, respectively. As shown in the figures, the blocking

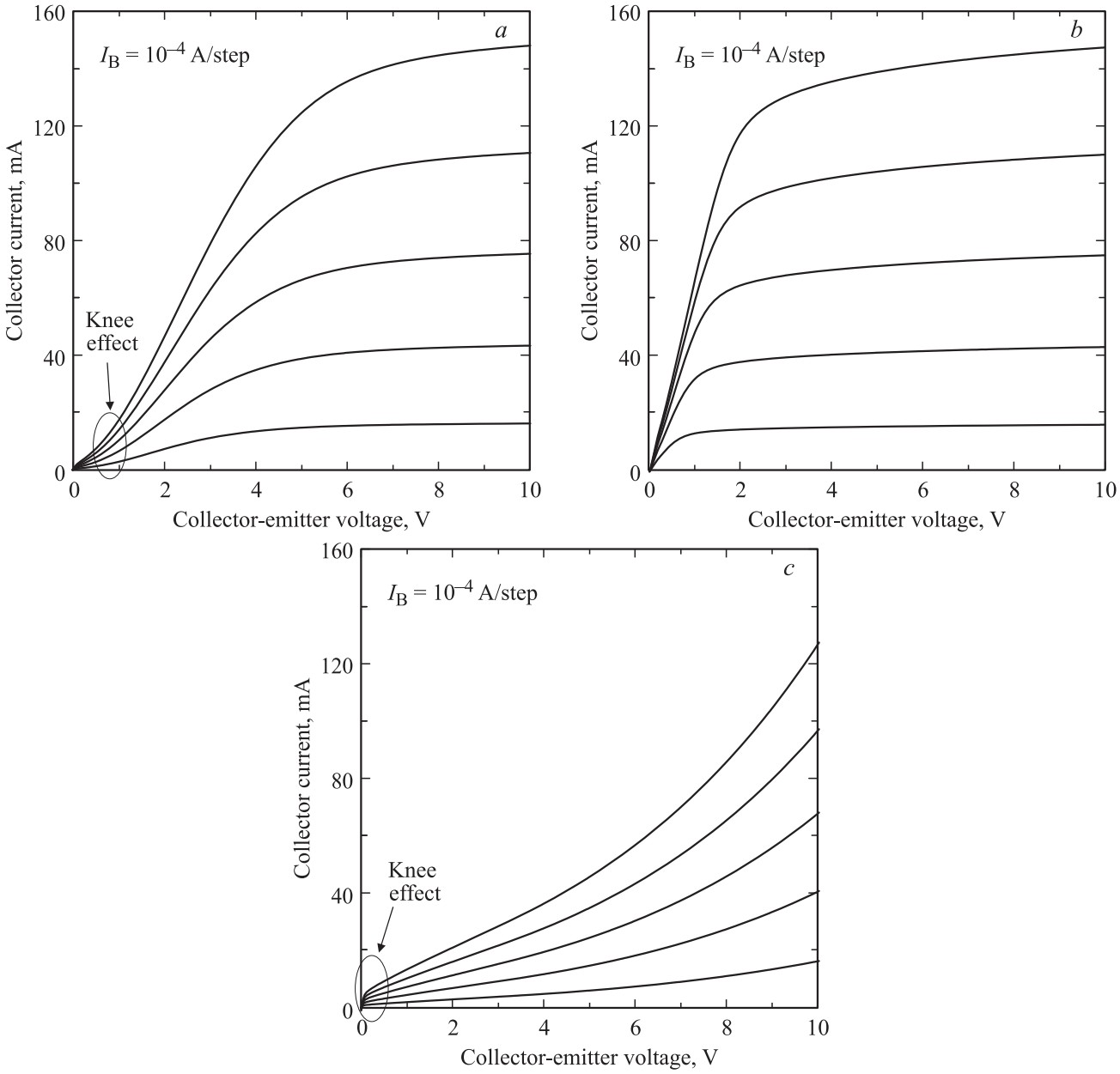

Figure 4. Common-emitter current-voltage characteristics of (*a*) device A, (*b*) device B, and (*c*) device C.

effect of the carrier transporting can be clearly depicted and explained by the plots at $V_{BC} = 0$. In the three devices, the ideality factors n_c of collector currents are nearly equal to unity at low current level. This means that the diffusion mechanism dominates the electron transportation across the B-E junction. In addition, the ideality factors of base currents n_b at low current level are of about 1.33 in the three devices. This means that the employment of a thin InGsAsP spacer nearly does not affect the diffusion/recombination mechanism. In addition, when the spike is not lowered, the maximum current gains at $V_{BC} = 0$ are of 21.5, 123.2, and 5.29 in the devices A, B and C, respectively. Apparently, the addition of a 300 Å InGaAsP spacer layer substantially promotes the current gain than the other devices. The reason is mainly attributed that a thicker InGaAsP spacer layer can more effectively pull down the barrier (or spike) at B-C side.

4. Conclusion

In summary, unlike the conventional DHBT with relatively large potential spike at B-C junction, only two small spikes are formed and the current gains are greatly enhanced for the insertion of an InGaAsP spacer layer between base and collector layers. As comparing the three devices, the employed InGaAsP spacer layer could enable the current to effectively enhance. Furthermore, the thicker spacer layer

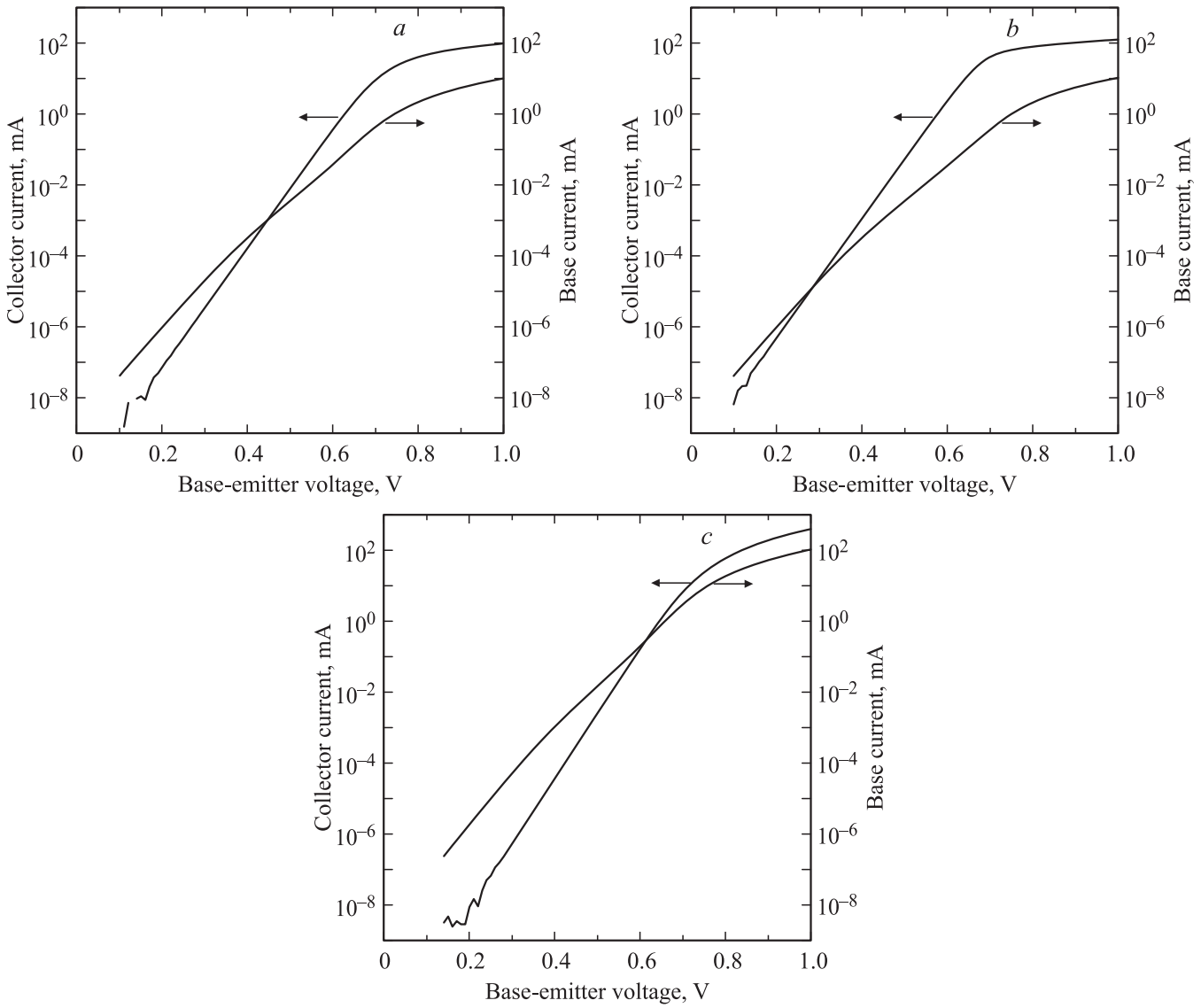

Figure 5. Simulated Gummel plots at $V_{BC} = 0$ of (*a*) device A, (*b*) device B, and (*c*) device C.

helps to reduce the blocking effect at B-C junction and eliminate the knee effect in *I-V* curves. Consequently, the studied InP/InGaAs DHBTs with InGaAsP spacer layer is promising for signal amplifier and circuit applications.

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