Analytical one-dimensional current–voltage model for FD SOI MOSFETs including the effect of substrate depletion

© Rahul Pandey, Aloke K. Dutta¶

Department of Electrical Engineering Indian Institute of Technology,
UP 208016 Kanpur India

(Получена 6 февраля 2013 г. Принята к печати 7 февраля 2013 г.)

In this paper, we present an analytical one-dimensional current–voltage model for silicon-on-insulator (SOI) MOSFETs under full depletion (FD). Our model has been developed from the first principles, and it not only includes the effects of source–drain series resistances, self-heating, and parasitic BJT, which are essential to FD SOI device modeling, but also includes another important effect of substrate depletion, for the first time in the literature, which is of vital significance for FD SOI devices having small film thickness and low substrate doping. The results of the drain current obtained from our model show a much better match with the experimental data, with the maximum error being only 9.41%, which is reasonably lower than the maximum error of 15.04% produced by the model of Yu et al., and marginally better than the error of 11.5% of the model of Hu and Jang. It must be noted that, though the improvements achieved in terms of accuracy are not that significant, yet unlike other models, ours is based on a simplified one-dimensional analytical approach, which is absolutely free from iterations, and hence, there is a huge improvement in terms of computational efficiency, which establishes its practical significance.

1. Introduction

With the increasing limitations encountered in CMOS technology, attempts have been made to realize transistor action not only by changing the device structure (e. g., FinFETs) but also by altering the current transport mechanism (e.g., spintronics). Whether a new technology will be able to thrive in the semiconductor industry or not depends greatly on its compatibility with the present technology. It has been found that silicon-on-insulator (SOI) MOSFETs, besides sharing certain structural similarities with the bulk MOSFETs, also offer significant advantages over them, viz., low parasitic capacitances and leakage currents, better resistance against the short channel effects [1], improved subthreshold swing [2], etc.

Out of the two categories of SOI MOSFETs, i. e., partially-depleted (PD) and fully-depleted (FD), the latter has been the key focus of SOI device modeling due to their improved electrical characteristics as compared to the former [1,2]. Hsiao et al. [3] and Hu and Jang [4] proposed current-voltage models specifically for the FD SOI MOSFETs. However, while the former failed to take into account the effect of the self-heating [5], the latter did not incorporate the parasitic BJT effect [6], which resulted in incomplete modeling, and hence, produced significant errors.

Additionally, FD SOI MOSFETs show existence of a depletion region in the silicon substrate too, which is especially important for thin film SOI devices (which are gaining popularity due to their better control over the short channel effects [1]) having lowly doped substrates [7]. In 2008, Agarwal et al. [7] included this effect of substrate depletion for the first time, in estimating the surface potential for the FD SOI MOSFETs. Yet, an analytical model that admits this effect in determining the current-voltage characteristics is still lacking in the literature.

¶ E-mail: aloke@iitk.ac.in

Hence, the goal of our work is to develop a simplified analytical current–voltage model, specifically for the FD SOI devices, which not only includes the effects of source-drain series resistance, self-heating, parasitic BJT, etc., which are important in modeling the behavior of FD SOI MOSFETs in present day technology, but also incorporates the effect of substrate depletion for the first time in modeling of the current–voltage characteristics of FD SOI MOSFETs. It will be shown that our current–voltage model, though one-dimensional and purely analytical, achieves reasonably good accuracy.

The work is presented in the following sequence. The model development is presented in Section 2, with subsections 2.1, 2.2, 2.3, and 2.4 detailing the models for the inversion charge, the carrier mobility in the channel of an SOI MOSFET, the current-voltage model in strong inversion, and the improvement in the model, respectively. The results are discussed in Section 3, while the summary and conclusion are presented in Section 4.

2. The current–voltage model

In this section, we attempt to develop a one dimensional current–voltage model for FD SOI MOSFETs, employing the assumption of pinning of the surface potential in strong inversion. This approach, in combination with the gradual channel approximation, will not only help in incorporating the effect of substrate depletion easily [7], but also will result in a simplified model. Majority of current–voltage models available in the literature follow a two-dimensional approach, which involves definitions of complex terms and intricate analyses, increasing computational overheads [4,8,9]. It will be shown that the current–voltage model developed in this work, achieves remarkable accuracy, while preserving its analytical one-dimensional nature.

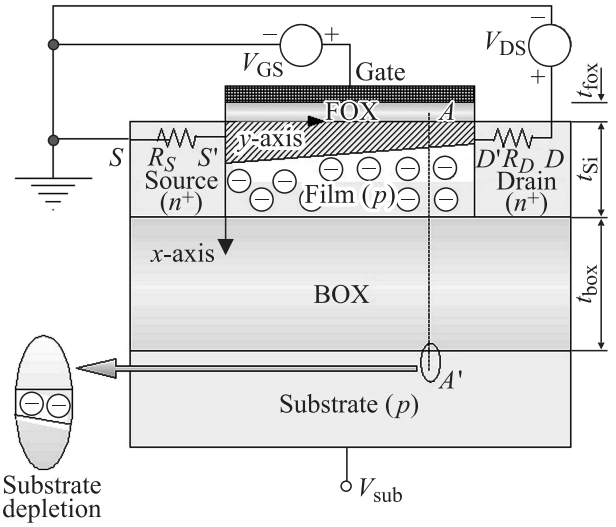

Figure 1. An *n*-channel FD SOI MOSFET operating in strong inversion. All terminal voltages are referred to source, which is grounded.

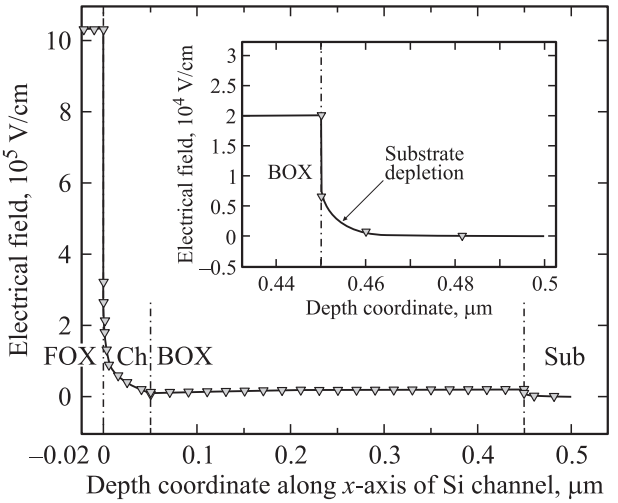

Figure 2. Electric field along the *x*-axis, at around the middle of the Si channel, for an FD SOI MOSFET, simulated in MEDICI. FOX-channel interface is taken as the origin for the *x*-axis. Inset: A magnified view at the substrate-BOX interface. Note the changed scale for the *y*-axis. Substrate depletion is clearly visible here. Device parameters: $L = 300$ nm, $N_{ch} = 10^{17}$ cm^{-3}, $N_{sub} = 10^{18}$ cm^{-3}, $t_{Si} = 50$ nm, $t_{fox} = 20$ nm, and $t_{box} = 400$ nm.

Fig. 1 shows a typical *n*-channel FD SOI MOSFET, operating in strong inversion. The substrate voltage V_{sub} is made equal to the back surface flatband voltage V_{FB} in order to ensure that the current conduction in the channel is governed solely by the gate. Due to the existence of parasitic source and drain series resistances (R_S and R_D respectively), intrinsic source and drain terminals (S' and D' respectively) are defined, which are located on either side of the channel, and are different from the physically accessible extrinsic source and drain terminals, denoted by S and D respectively in the same figure.

Fig. 1 also illustrates the phenomenon of substrate depletion, which is a consequence of a rise in the gate voltage beyond the point at which the silicon film gets fully depleted. This effect is conspicuous from the MEDICI simulation of a thin film FD SOI MOSFET, as shown in Fig. 2, which plots the electric field profile along a vertical cross-section (i.e., along the *x*-axis), located somewhere around the middle of the silicon channel for a representative device, with all required data given in the figure caption. The region of positive electric field existing in the substrate, near the substrate-BOX interface, marks the extent of depletion produced in it.

Substrate depletion is important for thin film SOI devices, which is aggravated further by low substrate doping [7]. If the substrate depletion charge is neglected, then the inversion charge in the fully depleted case will be overestimated, and will thus result in a higher value of the channel current. To the best of our knowledge, this effect has never been included in the analysis of the current-voltage model for FD SOI MOSFETs, and hence, an important goal of this work is to incorporate this effect. Small dimension effects, e.g., carrier velocity saturation, high-field effects, and parasitic source–drain series resistances, too will be covered in detail during the development of our model. Finally, the effects of parasitic BJT and lattice heating will also be included, which will result in a complete and thorough analytical current–voltage model for FD SOI devices.

2.1. Model for the inversion charge

The development is initiated by following the standard procedure of writing the potential balance and charge balance expressions along a vertical cross-section (e.g., A–A') of the FD SOI MOSFET, as shown in Fig. 1. It is assumed that this chosen cross-section is sufficiently away from the channel end points, so as to avoid the edge effects [10]. Using the potential balance and charge balance equations [10,11], the inversion charge per unit area Q'_1 can be expressed as:

$$Q'_I = -C'_{fox}\left[V_{GB} - V_{FF} - \psi_{sf} + \frac{Q'_B + Q'_{subs}}{C'_{fox}}\right], \qquad (1)$$

where $C'_{fox} = \varepsilon_{ox}/t_{fox}$, with ε_{ox} and t_{fox} being the permittivity of SiO_2 and the front oxide thickness respectively, is the front oxide capacitance per unit area, V_{GB} is the gate voltage, referred to an imaginary neutral body [11] (note here that during the course of the analysis, the reference of the model will be transferred to the source, which in turn, is grounded), V_{FF} is the front gate flatband voltage, ψ_{sf} is the front surface potential of the Si film, and Q'_B and Q'_{subs} are the depletion charges per unit area in the film and in the substrate respectively.

Since it is commonly assumed that ψ_{sf} gets pinned at strong inversion, it can be approximated as [10]:

$$\psi_{sf} = 2\varphi_F + n\phi_t + V_{CB}(y) = \phi_0 + V_{CB}(y), \quad (2)$$

where $\phi_0 = 2\phi_F + n\phi_1$, and $\phi_F = \phi_t \ln(N_{ch}/n_i)$, with ϕ_t being the thermal voltage, N_{ch} is the channel doping concentration, and n_i, is the intrinsic carrier concentration of Si, is the bulk potential of the Si channel, $V_{CB}(y)$ is the channel to bulk potential (corresponds to the splitting of the Fermi levels in these two regions), and n is a constant, with its value typically ranging between 4 and 6 [10].

Under full depletion, Q'_B is a constant, dictated only by N_{ch} and the channel thickness t_{Si}, $[Q'_B = -qN_{ch}t_{Si}]$, while Q'_{subs} is related to the band bending in the substrate ψ_{subs} as $Q'_{subs} = -\gamma_{subs}C'_{box}\sqrt{\psi_{subs}}$, where $\gamma_{subs} = \sqrt{2q\varepsilon_s N_{subs}}/C'_{box}$, with ε_s being the permittivity of Si, N_{subs} is the substrate doping, $C'_{box} = \varepsilon_{ox}/t_{box}$, with tbox being the box oxide thickness is the box oxide capacitance per unit area. ψ_{subs} in strong inversion can be estimated as [7]:

$$\psi_{subs} = \left(-B + \sqrt{B^2 - \alpha + \psi_{sf}}\right)^2 \quad (3)$$

where $B = 0.5\gamma_{subs}(1 + C'_{box}/C'_{Si})$, with C'_{Si} $(= \varepsilon_s/t_{Si})$ being the Si channel capacitance per unit area, and $\alpha = qN_{ch}t_{Si}^2/(2\varepsilon_s)$, where q is the Coulomb charge. From Eqs. (2) and (3), we get:

$$Q'_{subs} = -\gamma_{subs}C'_{box}\left(-B + \sqrt{D + V_{CS}(y)}\right), \quad (4)$$

where $D = B^2 - \alpha + \phi_0 + V_{SB}$, with V_{SB} being the source-to-body voltage. Finally, in order to obtain the expression for the inversion charge, Eqs. (1), (2), and (4) are used to get:

$$Q'_I = -C'_{fox}\left[V_{GS} - V_T - V_{CS}(y) - \gamma'\left(-B + \sqrt{D + V_{CS}(y)}\right)\right], \quad (5)$$

where V_{GS} is the gate-to-source voltage, and

$$V_T = V_{FF} + \phi_0 + \frac{qN_{ch}t_{Si}}{C'_{fox}} \quad (6)$$

with $\gamma' = \gamma_{subs}C'_{box}/C'_{fox}$. Though the term V_T expressed by Eq. (6) is rigorously not the threshold voltage of the device, still its value matches so closely with the actual threshold values predicted by the two dimensional analysis [4,8], for typical values of device parameters as used in [4,8,12], that it can be treated as the threshold voltage for all practical purposes. Typical range of threshold voltage for a device having dimensions similar to that used in our model, for channel doping of $10^{16}-10^{17}\,cm^{-3}$, is around 0.1–0.4 V. We will assume that the change in the threshold voltage with respect to temperature remains negligible.

The term $V_{CS}(y)$ appearing in Eq. (5) can be related to the channel-intrinsic source potential $V_{CS'}(y)$ [please refer to Fig. 1], assuming that the direction of the current entering the drain terminal is positive, as $V_{CS}(y) = V_{CS'}(y) + I_{DS}R_S$, where I_{DS} is the drain-to-source current in strong inversion. Thus, Eq. (5) gets modified as:

$$Q'_I = -C'_{fox}\left[V_{GST} - V_{CS'}(y) - \gamma'\left(-B + \sqrt{D + V_{CS}(y)}\right)\right] + C'_{fox}I_{DS}R_S, \quad (7)$$

where $V_{GST} = V_{GS} - V_T$. In Eq. (7), the $V_{CS}(y)$ term under the square root sign has been kept intact, as this extrinsic source reference automatically gets eliminated during the course of further analysis, as will be shown later.

2.2. Carrier Mobility in SOI MOSFETs

Besides surface roughness scattering, carrier mobility in SOI MOSFETs is influenced by three other major factors, namely lattice heating, carrier mobility degradation due to high gate field, and carrier velocity saturation. Out of these three, lattice heating is of crucial importance here as compared to the case of bulk MOSFETs [5]. This is due to the presence of the buried oxide just beneath the channel, which being an insulator, poses a huge bottleneck in terms of its heat sinking capability. The temperature dependence of mobility is empirically expressed as [6]:

$$\mu_0 = \mu_{amb}\left(\frac{T_{amb}}{T_0}\right)^Z \quad (8)$$

where μ_0 and μ_{amb} are the maximum values of the low-field carrier mobility in the inversion channel, at temperatures T_0 (of lattice) and T_{amb} (of ambient) respectively. In Eq. (8), Z is an empirical coefficient, and in the literature, its value has been reported to be in the range from 1.2 to 2 [10]. In this work, a value of 2 for Z has been used, based on the suggestion of recent works [12,13].

The carrier mobility degradation due to the vertical gate field can be modeled as [6]:

$$\mu_{n0} = \frac{\mu_0}{1 + \theta V_{GST}}, \quad (9)$$

where μ_{n0} is the carrier mobility at a given V_{GS}, and the mobility degradation parameter θ is estimated by the empirical approximation $\theta = \beta_\theta/t_{fox}$ [14], where β_θ is yet another fitting parameter, with its value ranging from 0.5 to 2 nm/V [14]. Finally, in order to account for the effect of carrier (electron) velocity saturation, we use the model reported in [15], use Eq. (2), and change variable V_{CS} to $V_{CS'}$, thus yielding:

$$\mu_n(y) = \frac{\mu_{n0}}{1 + \frac{\mu_{n0}}{v_{sat}}\frac{dV_{CS'}(y)}{dy}}, \quad (10)$$

where v_{sat} is the saturation velocity for electrons, which again is temperature dependent. This will be discussed further in sub-section 2.4.

2.3. Current-voltage model in strong inversion

Using the drift–diffusion model, the channel current I_{DS} is given by [10]:

$$I_{DS} = W\mu_n(y)\left[-Q'_I(y)\frac{d\psi_{sf}(y)}{dy} + \phi_t\frac{dQ'_I(y)}{dy}\right], \quad (11)$$

where W is the channel width. Using the expressions for inversion charge and carrier mobility from Eqs (7) and (10), Eq. (11) gets expressed as:

$$\frac{I_{DS}}{W\mu_{n0}}\left[1+\mu_{n0}\left(\frac{1}{\upsilon_{sat}}+WC'_{fox}R_S\right)\frac{dV_{CS'}(y)}{dy}\right] = C'_{fox}\left[V_{GST}-V_{CS'}(y)-\gamma'\left(-B+\sqrt{D+V_{CS}(y)}\right)\right] \times\frac{dV'_{CS}(y)}{dy}+\phi_t\frac{dQ'_I(Y)}{dy}. \quad (12)$$

Integrating both sides of Eq. (12) along the channel, i. e., from $y = 0$ to $y = L$, where L is the channel length, and then simplifying by making use of binomial approximations, we get:

$$I_{DS} = \frac{H\left[V_{GST\eta}-\frac{V_{D'S'}}{2}\right]V_{D'S'}}{L+\left(\frac{\mu_{n0}}{\upsilon_{sat}}+HR_S\right)V_{D'S'}}, \quad (13)$$

where $H = W\mu_{n0}C'_{fox}$, $V_{GST\eta} = V_{GST} - \eta$, with

$$\eta = \frac{\gamma'\delta}{2B}-\varphi_t\left(1+\frac{\gamma'}{2\sqrt{D}}\right), \quad (14)$$

where $\delta = \varphi_0 - \alpha + V_{SB}$.

Note that Eq. (13) represents I_{DS} as a function of the intrinsic drain-source voltage $V_{D'S'}$, which is related to the extrinsic (or terminal) drain-source voltage V_{DS} by $V_{D'S'} = V_{DS} - I_{DS}R_T$, where $R_T = R_S + R_D$ is the total series resistance of the device. Using this substitution in Eq. (13). We get a quadratic expression in terms of I_{DS}, the solution of which is given by:

$$I_{DS} = \frac{-P_1-\sqrt{P_1^2-4P_2P_0}}{2P_2}, \quad (15)$$

where

$$P_2 = \frac{HR_T(R_S-R_D)}{2}+\frac{R_T\mu_{n0}}{\upsilon_{sat}} \quad (16)$$

$$P_1 = -HR_T\left(V_{GST\eta}-\frac{V_{DS}R_D}{R_T}\right)-L-\frac{V_{DS}\mu_{n0}}{\upsilon_{sat}} \quad (17)$$

and

$$P_0 = H\left(V_{GST\eta}-\frac{V_{DS}}{2}\right)V_{DS}. \quad (18)$$

The drain-to-source saturation voltage V_{DSsat} can be obtained by equating the slope dI_{DS}/dV_{DS} to zero, thus yielding:

$$V_{DSsat} = \frac{-G_1+\sqrt{G_1^2-4G_2G_0}}{2G_2}. \quad (19)$$

with

$$G_2 = H\Gamma^2[2u+H(R_s-R_D)]R_T, \quad (20)$$

$$G_1 = 2HR_T(\Gamma+1)(L-HR_TV_{GST\eta}\Gamma) \quad (21)$$

and

$$G_0 = (HR_TV_{GST\eta}\Gamma-L)^2-(HR_TV_{GST\eta}+L)^2, \quad (22)$$

where $u = \mu_{n0}/\upsilon_{sat}$, and $\Gamma = (u+HR_S)/(u-HR_D)$. Using Eqs (15) and (19), the drain–source saturation current I_{DSsat} is given as:

$$I_{DSsat} = \frac{V_{GST\eta}-V_{DSsat}}{\frac{u}{H}-R_D}. \quad (23)$$

Equations (15)–(18) express our basic current–voltage model for FD SOI n-channel MOSFETs operating in strong inversion. The remaining task is to refine the model, by including some other important second-order effects, as presented in the following section.

2.4. Improvement in the current–voltage model

We have already taken into account the effects of carrier velocity saturation and parasitic source-drain series resistance in our model. However, in order to improve the accuracy of the model, consistent with suggestions made in the literature [5,15], we include some other important second–order effects, namely channel length modulation (CLM), self-heating, and parasitic BJT action.

The CLM effect can be modeled by replacing the drawn channel length L by an effective channel length $L_{eff} \equiv L - \Delta L$, where ΔL is the reduction in the channel length due to this effect, which takes care of the modulated part of the channel [12,15]. We have included this effect by approximating ΔL due to CLM as [10]:

$$\Delta L = l_a \ln\left[1+\frac{V_{DS}-V_{DSsat}}{V_E}\right] \quad (24)$$

where l_a is the characteristic length, empirically expressed as $l_a \simeq (0.22\,\mathrm{cm}^{1/6})d_j^{1/2}t_{ox}^{1/3}$, with d_j being the drain junction depth, and $V_E \approx 0.1$ V is determined from the best fit with experimental data [10].

In order to model the self-heating effect, we note that the difference between the lattice temperature T_0 and ambient temperature T_{amb} is linearly proportional to the power dissipated $P_{diss} = V_{DS}I_{DS}$ in the device [9,16], i. e., $T_0 - T_{amb} = R_{th}V_{DS}I_{DS}$, where R_{th} is the proportionality constant, known as the thermal resistance of the device, given by [5,13]:

$$R_{th} \simeq \frac{1}{W}\left(\frac{t_{box}}{K_{ox}K_dt_{Si}}\right)^{1/2}, \quad (25)$$

where K_{ox} and K_d are the thermal conductivities of SiO_2 and n^+-Si source-drain regions respectively. Thus, we can now express μ_{n0} [Eq. (9)] at the lattice temperature T_0 in terms

of the carrier mobility μ_{na} at the ambient temperature T_{amb} as:

$$\mu_{n0} = \mu_{na}(1 + AV_{DS}I_{DS})^{-2} \quad (26)$$

where $\mu_{na} = \mu_{amb}/(1 + \theta V_{GST})$ and $A = R_{th}/T_{amb}$. Note that for typical thin film SOI devices, with tbox around 400 nm and t_{Si} around 90 nm or less, $R_{th} \approx 10^4$ K/W. Also, since typically P_{diss} is of the order of mW, hence, the product term $AV_{DS}I_{DS}$ in Eq. (26) is of the order of 10^{-2}, which makes the use of binomial approximation possible. Thus, replacing μ_{n0} in terms of μ_{na} from Eq. (26) in Eqs (16)–(18) along with including the CLM effect, the coefficients in Eq. (15) get updated to:

$$P_2 = \frac{WC'_{fox}R_T(R_S - R_D)}{2} + \frac{R_T}{v_{sat}} - \frac{2AL_{eff}V_{DS}}{\mu_{na}} \quad (27)$$

$$P_1 = -W^*C'_{fox}R_T\left(V_{GST\eta} - V_{DS}\frac{R_D}{R_T}\right) - \frac{L_{eff}}{\mu_{na}} - \frac{V_{DS}}{v_{sat}} \quad (28)$$

and

$$P_0 = WC'_{fox}\left(V_{GST\eta} - \frac{V_{DS}}{2}\right)V_{DS}. \quad (29)$$

The updated expression for P_2 has a V_{DS} dependence, which makes the derivation of V_{DSsat} difficult, as now the equation for V_{DSsat} will turn cubic. Still the expression for V_{DSsat} given by Eq. (19) can be used, which yields an average error of only 6.4%, based on the results obtained from our simulations. In order to obtain better accuracy, one can either opt for an iterative solution or go for an empirical fitting for simplicity. For example, for the device technology employed in our simulations, as given in the Table, the following relationship was extracted by us for V_{DSsat}, after verification with the experimental data reported in [12]:

$$V_{DSsat} = \xi V_{GST\eta} + 8\phi_t \quad (30)$$

where ξ is an empirical fitting parameter with a value of 0.66. Equation (30) predicts V_{DSsat} with a maximum error of only 1.8% (to be discussed in detail later in the Results section), which is reasonable and a decent alternative to avoid iterations.

As mentioned at the end of sub-section 2.2, the saturation velocity for electrons v_{sat} is also temperature dependent. At any temperature T_0, this dependence is expressed as [17]:

$$v_{sat} = \frac{v^*}{1 + C\exp(T_0/\Theta)}, \quad (31)$$

where $v^* = 2.4 \cdot 10^7$ cm/s, $C = 0.8$ and, $\Theta = 600$ K. However, inclusion of the temperature dependence of v_{sat}, expressed in the form of Eq. (31), makes our model equations for the drain current transcendental in nature. As our goal is to build a model that is free from any kind of iterations, hence, attempt is now being made to obtain a simplified expression for v_{sat} by making use of reasonable approximations.

Considering the effect of self-heating, the exponential term in the denominator of Eq. (31) can be written as: $C\exp(T_0/\Theta) \approx C\exp[(T_{amb} + R_{th}V_{DS}I_{DS})/\Theta] = C\exp[(1 + AV_{DS}I_{DS})/2]$, since $\Theta = 2T_{amb}$. Now, since typical devices have power dissipation P_{diss} in the order of mW, the product term $AV_{DS}I_{DS}$ is of the order of 10^{-2}, as has been discussed earlier. This eventually gives us a very compact expression for v_{sat} as $v_{sat} \approx v^*/[1 + C\exp(0.5)] = 1.1 \cdot 10^7$ cm/s, which is used in our model as the nominal value of v_{sat}, under the assumption that P_{diss} of the device is in the order of mW. For higher values of P_{diss}, v_{sat} can be determined using the iterative approach.

Finally, the expression for the total drain current, that includes the effects of impact ionization and parasitic BJT, is given by [6,9]:

$$I_D = GI_{DS} + FI_{CBO}, \quad (32)$$

where

$$G = 1 + \frac{(M-1)[1 - (1-K)\alpha_0]}{1 - [1 + KK'(M-1)]\alpha_0}, \quad (33)$$

$$F = \frac{1 + K'(M-1)}{1 - [1 + KK'(M-1)]\alpha_0} \quad (34)$$

and

$$M - 1 = \beta_1(V_{DS} - V_{DSsat})\exp\left(-\frac{\beta_2}{V_{DS} - V_{DSsat}}\right), \quad (35)$$

where the parameter K is a fraction of the impact ionization hole current, driven by the vertical gate field towards the BOX, while K' denotes a similar fraction of the collector electron current, directed towards the high electric field region near the drain end of the channel [6]. The parameter M is the multiplication factor. The fitting parameters β_1 and β_2 are process dependent, and insensitive to temperature variations [18,19]. The term α_0 relates the collector and the emitter currents, I_C and I_E respectively, of the parasitic BJT as:

$$I_C = \alpha_0 I_E + I_{CBO}, \quad (36)$$

where I_{CBO} is the leakage current across the collector–base (for our case, it is the drain–body) junction, with the emitter–base (i.e., source–body) junction open circuited. It depends on V_{GST} as [20]:

$$I_{CBO} = \frac{WT_{Si}I_{so}}{1 + \lambda V_{GST}} \quad (37)$$

with I_{so} being the leakage current per unit cross-sectional area of the collector–base junction, and λ is a fitting parameter having a dimension of V^{-1}.

Now, during the onset of saturation, i.e., as V_{DS} approaches V_{DSsat}, $M \to 1$, which makes $G \to 1$, while $F \to F_0$, where $F_0 = (1 - \alpha_0)^{-1}$. Thus, the drain current at this instant can be expressed as:

$$I_D = I_{D0} = I_{DS} + F_0 I_{CBO}. \quad (38)$$

In fact, Eq. (35) is meaningful only from the onset of saturation and beyond, so that the multiplication factor M

The values of parameters used in simulations

Parameter (Unit)	Value	Parameter (Unit)	Value	Parameter (Unit)	Value	Parameter (Unit)	Value
$W(\mu m)$	7.83	$L(\mu m)$	0.28	$N_{ch}\,(cm^{-3})$	10^{16}	$N_{subs}\,(cm^{-3})$	10^{18}
$t_{Si}(nm)$	94	$t_{fox}(nm)$	10	$t_{box}(nm)$	347	$R_S,\ R_D(\Omega)$	70
$\mu_{amb}\,(cm^2/V\cdot c)$	670	$v_{sat}\,(m/s)$	$1.1\cdot 10^5$	$\theta(V^{-1})$	0.05	$Z(-)$	2.0
$K,\ K'(-)$	0.85	$K_d\,(W/m\cdot K)$	63	$K_{ox}\,(W/m-K)$	1.4	$\beta_1(V^{-1})$	0.3
$\beta_2\,(V)$	13	$\alpha_0(-)$	0.994	$\lambda(V^{-1})$	2.0	$I_{so}\,(A/cm^2)$	80
$m_1(-)$	1.0	$m_2(-)$	1.0	$T_{amb}\,(K)$	300		

is always ≥ 1. Hence, there is a need to unify the pre-saturation current I_{DS}, which is still given by Eq. (15), with the updated coefficients from Eqs (27)–(29) to the post-saturation current I_D, expressed by Eq. (32). This can be achieved by using the following standard smoothing function, involving exponentials:

$$I_{ch}=\frac{I_{DS}}{1+m_1\exp\left(\frac{V_{DS}-V_{DSsat}}{m_2\phi_t}\right)}+\frac{I'_D}{1+m_1\exp\left(-\frac{V_{DS}-V_{DSsat}}{m_2\phi_t}\right)}, \tag{39}$$

where I_{ch} is the unified channel inversion current, while m_1 and m_2 are fitting parameters. Note that since I_D was not defined for $V_{DS} < V_{DSsat}$, and because the smoothing function requires each participating function to have meaningful values over the entire range of V_{DS}, hence, a function I'_D [appearing in Eq. (39)] is defined in order to achieve the goal of unification, expressed as:

$$I'_D=\begin{cases} I_{D0} & \text{for } V_{DS}\leq V_{DSsat} \\ I_D & \text{for } V_{DS}> V_{Dssat} \end{cases}. \tag{40}$$

Thus, instead of using I_D, we use I'_D from Eq. (40), which is defined for all values of V_{DS}, in order to evaluate the final channel current I_{ch} by using Eq. (39).

3. Results

The results obtained from the channel current (I_{ch}) model developed in this work [Eq. (39)] were compared with the experimental data reported in the literature [4,12]. The device used in the simulations has dimensions of prevalent technology standards, as illustrated in Table. In Fig. 3, the variation of I_{ch} with respect to V_{DS} is plotted, with V_{GST} as the parameter. In the same figure, we also show the experimental data reported in [4], as well as the model results obtained from [4] and [12]. The match of our results with the experimental data is quite good, over almost the entire range of bias voltages.

In the saturation region, the impact ionization and the parasitic BJT effects are more pronounced for small gate voltages, as described in [9], which can also be observed from Fig. 3. Thus, there is a rise in the channel current as the drain bias is increased for $V_{GST} = 1$ V, because the contribution of the parasitic BJT (active underneath the inversion layer) towards the channel current is significant [6] due to the low gate field.

From the figure, it can also be noted that the results obtained from the model given in [4] deviate significantly from the experimental results at high drain bias for $V_{GST} = 1$ V. This is because [4] does not take into account the parasitic BJT effect, which is important at such bias conditions [6]. This produces a maximum error of 11.5% in the prediction of the drain current given by [4], for the range of drain voltage used in our simulation ($V_{DS} \leq 3$ V). As the parasitic BJT effect becomes more and more significant with the increasing drain bias [9], the error in the prediction of the drain current by [4] will definitely rise from this value (11.5%) as the drain voltage is increased further.

As compared to [4], the maximum error in our model for the same range of drain voltage is 9.41%, which lies within the accepted norm of 10% error band, and it will not grow with increasing drain bias, since our model incorporates the parasitic BJT effect too. Besides this, it should be noted that the model given in [4] is based on a two-dimensional approach, and thus, it has

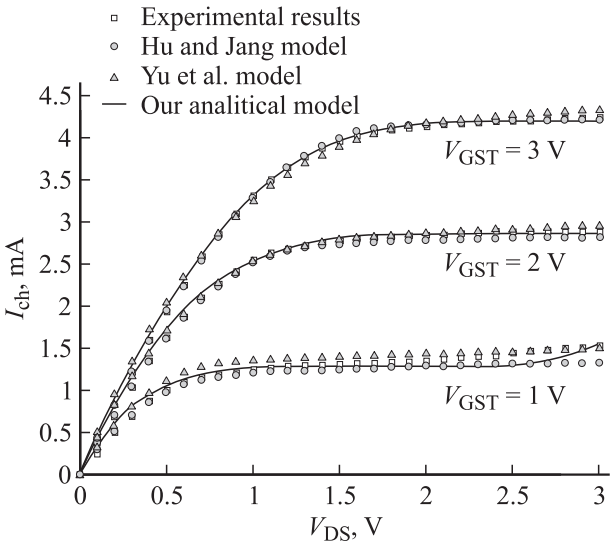

Figure 3. The channel current (I_{ch}) as a function of V_{DS}, for V_{GST} of 1, 2, and 3 V. The experimental data reported in [4] as well as the simulated results of [4] and [12] are also shown. The device data are listed in Table.

much more computational overheads as compared to our one-dimensional model. Hence, our model has superior characteristics as compared to [4]. From the figure, it is also clear that the results of [12] overestimates the channel current almost everywhere, for $V_{GST} = 1$ V. Hence, because of this overestimation, the maximum error of this model is 15.04%, which is quite higher than the error of 9.41% in the case of our model.

Besides improvement in terms of accuracy, we have included the effect of substrate depletion in our current-voltage model, which ensures that the channel current never gets overestimated due to the neglect of the substrate depletion charge. Note that the effect of substrate depletion becomes more pronounced for thin film SOI devices for increasing gate field. This fact is brought out beautifully in Fig. 3 (for $V_{GST} = 2$ and 3 V), where the results of our model match almost exactly with the measured data, whereas the results of the other two models [4,12] clearly either overestimate the on-state channel current or predict its behavior inaccurately. Hence, our model captures the essence of substrate depletion quite successfully. A lower substrate doping would only aggravate this phenomenon, which too has been accounted for in our model. Additionally, our model is purely analytical and simple as it avoids the two-dimensional analysis altogether, which increases its computational efficiency, while maintaining proper physical interpretations of the terms used in its derivation.

Next, we illustrate the accuracy achieved in the modeling of V_{DSsat}, both by the quadratic solution, i. e., using Eq. (19), and by the empirical approach, given by Eq. (30). Fig. 4 plots the variation of V_{DSsat} as a function of V_{GST}, with values obtained from three sources: experimental results [4], quadratic solution [Eq. (19)], and the empirical fit [Eq. (30)]. Fig. 5 plots the percent error in the prediction of V_{DSsat}, with respect to the experimentally obtained value of V_{DSsat} [4], by both the quadratic approach and the empirical approach, for each value of V_{GST}.

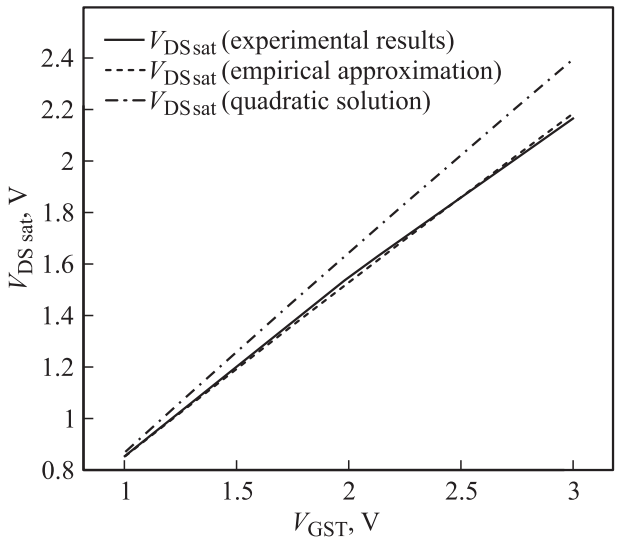

Figure 4. The drain–source saturation voltage (V_{DSsat}) as a function of V_{GST}. The results obtained from the empirical approximation [Eq. (30)] and the quadratic solution [Eq. (19)] are also shown. The results obtained from the empirical approximation show almost a perfect fit with that obtained from the experimental data.

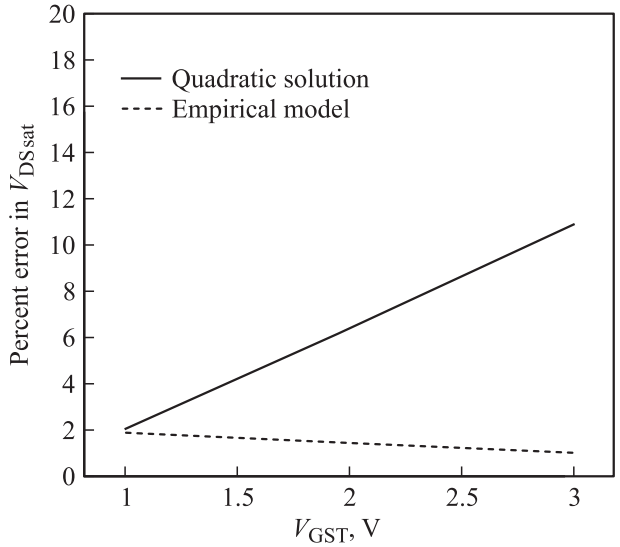

Figure 5. Percent error in V_{DSsat} as a function of V_{GST}. The error in the result obtained from the quadratic solution [Eq. (19)] increases linearly with V_{GST}, and reaches a maximum value of $\sim 10.86\%$ for $V_{GST} =$ V, while that obtained from the empirical model [Eq. (30)] shows very little variation with V_{GST}, and has a maximum value of only $\sim 1.86\%$.

From Figs. 4 and 5, it is found that the empirical model is better than the quadratic model, both in terms of accuracy as well as precision, as explained in the following discussion. The maximum error in predicting V_{DSsat} from the quadratic model is 10.86%, which is significantly higher as compared to the error of only 1.86% for the case of the empirical approach. Though due to the limited set of available experimental data, we could not map the parameter ξ in Eq. (30) to the device technology, still we emphasize the importance of the fact that such a fit can always be achieved.

4. Summary and conclusion

Since FD SOI MOSFETs are gaining popularity for integration into large scale designs as a substitute for bulk MOSFETs, due to their superior electrical characteristics as compared to their PD counterparts, we developed a drain current model, specifically for the FD SOI devices operating in the strong inversion region. Our model is based on a purely analytical and simplified one-dimensional approach. Besides incorporating the effects of source-drain series resistance, self-heating [5], and the parasitic BJT [6], which are essential non-idealities with regard to FD SOI modeling, our model also includes the effect of substrate depletion for the first time in the literature, in the derivation of the current-voltage characteristics for the FD SOI MOSFETs.

This effect is important for SOI devices having small film thickness and low values of substrate doping [7].

The results obtained from our current–voltage model have been compared with the experimental results from [4] and a remarkably good match is observed. We have also compared the results of our model with the predictions from two other models in the literature, namely that of Yu et al. [12] and Hu and Jang [4]. The maximum error produced by our model, with respect to experimental results, is 9.41%, which is reasonably lower than 15.04% in the case of Yu et al. model [12] and marginally better than 11.5% in the case of Hu and Jang model [4]. Though the amount of improvement achieved in terms of accuracy in our model with respect to Hu and Jang model [4] is not large, however, it must be noted that our model is one-dimensional, analytical, and absolutely free from any iterations, which would result in a significant savings in terms of computational overhead.

References

[1] Y.K. Choi, D. Ha, T.J. King, C. Hu. IEEE Electron. Dev. Lett., **22** (9), 447 (2001).
[2] J.P. Colinge. IEEE Electron. Dev. Lett., **7** (4), 244 (1986).
[3] T.C. Hsiao, N.A. Kistler, J.C.S. Woo. IEEE Electron. Dev. Lett., **15** (2), 45 (1994).
[4] M.C. Hu, S.L. Jang. IEEE Trans. Electron. Dev., **45** (4) 797 (1998).
[5] L.T. Su, J.E. Chung, D.A. Antoniadis, K.E. Goodson, M.I. Flik. IEEE Trans. Electron. Dev., **41** (1) 69 (1994).
[6] Y.G. Chen, J.B. Kuo, Z. Yu, R.W. Dutton. Sol. St. Electron. **38** (12) 2051 (1995).
[7] P. Agarwal, G. Saraswat, M.J. Kumar. IEEE Trans. Electron. Dev., **55** (3), 789 (2008).
[8] S.L. Jang, B.R. Huang, J.J. Ju. IEEE Trans. Electron. Dev., **46**, (9), 1872 (1999).
[9] M.C. Hu, S.L. Jang, Y.S. Chen, S.S. Liu, J.M. Lin. Jpn. J. Appl. Phys., **36**, 2606 (1997).
[10] Y.P. Tsividis. *Operation and Modeling of the MOS Transistor*, 2nd edn (Oxford University Press, 2008).
[11] H.K. Lim, J.G. Fossum. IEEE Trans. Electron. Dev., **30** (10), 1244 (1983).
[12] Y.S. Yu, S.H. Kim, S.W. Hwang, D. Ahn. IEE Proceedings–Circuits, Devices and Systems, **152** (2), 183 (2005).
[13] Y.G. Chen, S.Y. Ma, J.B. Kuo, Z. Yu, R.W. Dutton. IEEE Trans. Electron. Dev., **42** (5), 899 (1995).
[14] A.K. Dutta. *Semiconductor Devices and Circuits* (Oxford University Press, India, 2008).
[15] H.J. Park, P.K. Ko, C. Hu. IEEE Trans. Computer-Aided Design, **10** (3), 376 (1991).
[16] D.K. Sharma, J. Gautier, G. Merckel. IEEE J. Sol. St. Circuits, **13** (3), 378 (1978).
[17] C. Jacoboni, C. Canali, G. Ottaviani. A. Alberigi Quaranta. Sol. St. Electron., **20** (2), 77 (1977).
[18] W.N. Grant. Sol. St. Electron., **16** (10), 1189 (1973).
[19] S.M. Sze. *Physics of Semiconductor Devices*, 2nd edn (Wiley, N.Y., 1981).
[20] S. Bolouki, M. Maddah, A.A. Kusha, M.E. Nokali. Sol. St. Electron., **47** (11), 1909 (2003).

Редактор Т.А. Полянская