Dual Material Gate Engineering to Reduce DIBL in Cylindrical Gate All Around Si Nanowire MOSFET for 7-nm Gate Length

© *Sanjay , B. Prasad, A. Vohra*

Electronic Science Department, Kurukshetra University,
Kurukshetra-136119, Haryana, India

E-mail: sanjaykumarvlsi2015@gmail.com

Received July 6, 2020
Revised July 6, 2020
Accepted for publication July 17, 2020

In this work, drain current I_D for 7-nm gate length dual-material (DM) cylindrical gate all around (CGAA) silicon nanowire (SiNW) has been studied and simulation results are reported using Silvaco ATLAS 3D TCAD. In this device, we consider the non-equilibrium Green's function (NEGF) approach and self-consistent solution of Schrödinger's equation with Poisson's equation. The splitting of conduction in multiple sub-bands has been considered and there is no doping in the channel region. The effect of DM gate engineering (variation of screen gate and control gate length having different work function) for SiNW channel with 2-nm radius and gate oxide (SiO_2) thickness of 0.8 nm on I_D have been studied. It was found that DM gate engineering reduces drain-induced barrier lowering (DIBL) but it also slightly increases sub-threshold slope (SS). This work has obtained small DIBL (~ 54 mV/V), small SS (~ 68 mV/dec), and higher I_{On}/I_{Off} ($\sim 4 \cdot 10^8$) ratio as compared to literature concerning the inversion mode devices. The smallest DIBL is obtained when control gate length is the highest, and vice versa. With increase in control gate length, there is also increase in both I_{On} and I_{Off} but I_{On}/I_{Off} ratio decreases.

Keywords: NEGF, DM CGAA, inversion mode, SiNW, I_D, DIBL, SS.

Full text of the paper will appear in journal SEMICONDUCTORS.