Performance characteristics of p-channel FinFETs with varied Si-fin extension lengths for source and drain contacts

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The length of Source/Drain (S/D) extension (L_{SDE}) of nano-node p-channel FinFETs (pFinFETs) on SOI wafer influencing the device performance is exposed, especially in drive current and gate/S/D leakage. In observation, the longer L_{SDE} pFinFET provides a larger series resistance and degrades the drive current (I_{DS}), but the isolation capability between the S/D contacts and the gate electrode is increased. The shorter L_{SDE} plus the shorter channel length demonstrates a higher trans-conductance (G_m) contributing to a higher drive current. Moreover, the subthreshold swing (S.S.) at longer channel length and longer L_{SDE} represents a higher value indicating the higher amount of the interface states which possibly deteriorate the channel mobility causing the lower drive current.

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1. Introduction

In the present semiconductor industry exploring high-speed, low-cost, and high-volume capacity in IC products is the development trend. As entering the nano-node process generation, the FinFET structures are one of the impressive stars in the huge competitive devices. In the ON current for the short-channel n-channel MOSFETs (nMOSFETs), the Source/Drain (S/D) current at the saturation mode I_{DS} [1] can be demonstrated as:

$$I_{\text{DS}} = \frac{W_g}{L_g}\mu_n C_{\text{ox}}(V_{\text{GS}} - V_T)^2(1 + \lambda V_{\text{DS}}), \qquad (1)$$

where W_g — channel width, L_g — channel length, μ_n — mobility, C_{ox} — gate capacitance per area, V_{GS} — gate/source voltage, V_T — threshold voltage, and λ — channel length modulation factor.

For the FinFET structure, the general difficulties in device performance comprise the silicon fin (Si-fin) formation, gate stack, spacer isolation and Si-fin junction integrity [2–4]. These issues sometimes degrade the development speed. Considering the Si-fin structure, the benefit is to provide the longer channel width and the better gate controllability compared with the 2D MOSFETs, as shown in Fig. 1. The total channel width W_g is equal to the top side W_{fin} plus two times of H_{fin} at the side wall. Basically, the ratio of $H_{\text{fin}}/W_{\text{fin}}$ is greater than 8 or more to increase the drive current. However, the spacer integrity between the gate electrode and the contact part is easily suffered. In order to distinguish this concern, we design two Source/Drain extension lengths L_{SDE} as the gauge to probe this related electrical performance for the p-channel FinFETs.

2. Brief device fabrication

The SOI wafers [5–7] with 120 nm crystalline silicon (c-Si) layer were chosen and integrated with a traditional ULSI sub-65 nm generation logic technology to fabricate

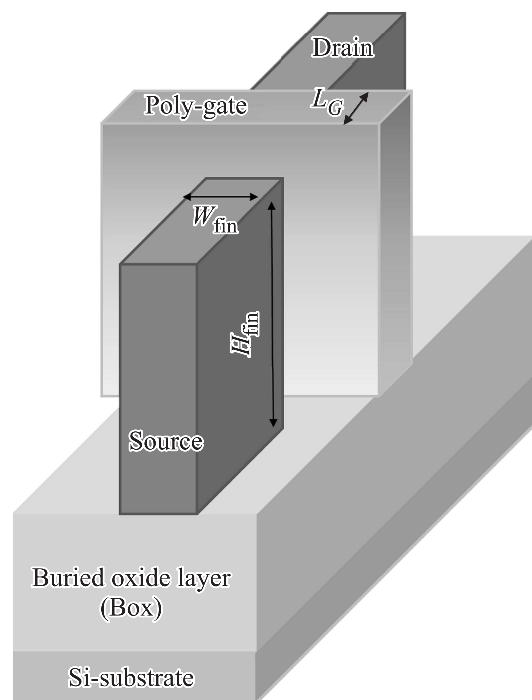

Figure 1. Schematic diagram of a FinFET device formed on the SOI wafer.

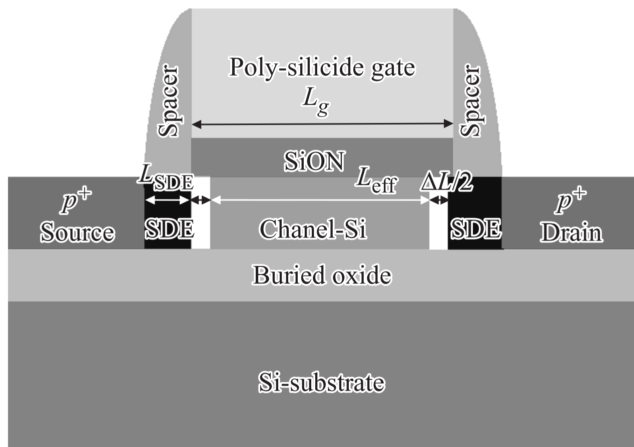

Figure 2. Schematic diagram of a p-channel FinFET observing from the Source/Drain region.

high aspect-ratio finFETs [8–11]. The p-channel FinFET devices were fabricated on this kind of SOI wafers. Using the oxidation-and-etch process steps incorporating the oxidation as well as the nitridation film as a hard mask, the top feature size of device on wafer can be controlled to $80-90$ nm or less. The final oxidation process was selected to achieve an adequate oxide layer for the subsequent Si-fin hard mask definition to get a desirable Si-fin width such as $11-27$ nm. A sacrificial thin oxide was followed to be grown on both sides of the vertical Si-fin sidewall to play as a screen oxide and to reduce the plasma-damaged thin Si-fin outer surface. Subsequently, boron (B) and arsenic (As) ions with a high tilted angle were doped for the threshold-voltage adjustment of n-channel and p-channel FinFET devices, respectively. After the threshold voltage (V_T) implantation, the screening oxide was removed, followed by the growth of a 14 Å (physical thickness) plasma nitrided oxide as the gate dielectric and an undoped $poly$-Si layer as the gate electrode. Subsequently, a high dosage phosphorus (P) was implanted for the NMOS and PMOS $poly$-Si gate area. After the gate spacer formation, both n^+ (As) and p^+ (B) source/drain ion implantations were conducted, followed by a Cobalt (Co) self-aligned silidation (salicidation) process [12] and a successive standard Tungsten (W) contact filling and Copper (Cu) interconnection. Eventually, a passivation layer was deposited, which is followed by the formation of aluminum bonding pads. The optimal aspect ratio for a single FinFET is about 8 at $H_{\text{fin}} = 90\,\text{nm} / W_{\text{fin}} = 17\,\text{nm}$ as the $poly$-Si gate channel length (L_g) shrunk to 30 nm. The simple diagram of a FinFET viewed from the Source/Drain region is represented in Fig. 2 [13].

3. Results and Discussion

Based on the need to increase the drive current, the high-k gate dielectric in FinFET [14–18] is gradually applied to fit the requirement of HPC IC products. However, the manufacturing cost is very expensive. Here, we just conduct the geometric change to enhance the drive current with the oxy-nitride gate dielectric. In this study, the tested device structure on the layout are $W_g/L_g = 0.11/0.5$, 2 and 10 (μm/μm) and the varied S/D extension lengths are 60 and 160 nm, respectively. Through the measurements, the current-voltage characteristics at $V_{\text{GS}}-V_T = -1$ V and the trans-conductance (G_m) curves at $V_{\text{DS}} = -0.05$ V are represented in Fig. 3 and 4, respectively. The subthreshold swing (S.S.) performance at $V_D = -0.05$ V is demonstrated in Fig. 5. Basically, the doping dosage at the S/D extension zone (P_{SDE}) is less than the S/D implant (P^+) around one tenth, compared with the lightly-doped drain implant (P^-) before 110 nm node process (normally, $\text{P}^+/\text{P}^- > 10$) to reduce the hot-carrier effect (HCE) [19–22]. Owing to this effort, the series resistance in channel is decreased and the ON current is possibly increased. The HCE causing the drain damage is little by little suppressed due

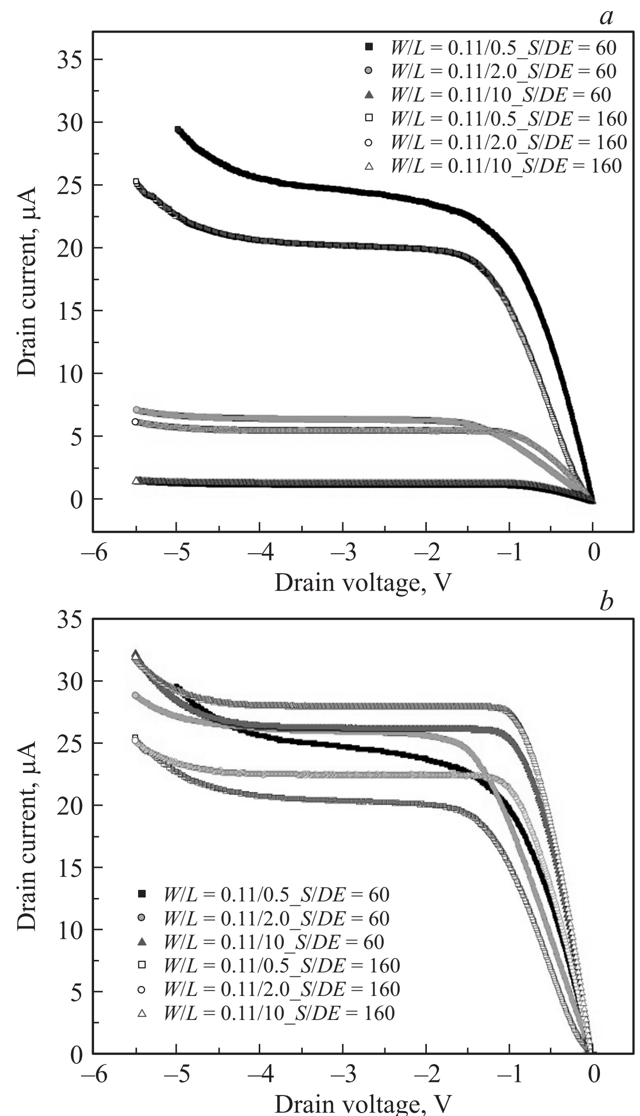

Figure 3. I_{DS} — V_{DS} curves: a — original measurement data and b — normalized data with the view of the identical channel length of $L_{\text{G}} = 0.5\,\mu$m defined by the $poly$-Si gate length.

to the lower supply voltage less than the creation of the required interface state energy (≥ 1.3 eV). The shorter L_{SDE} provides the lower series resistance contributing to the entire

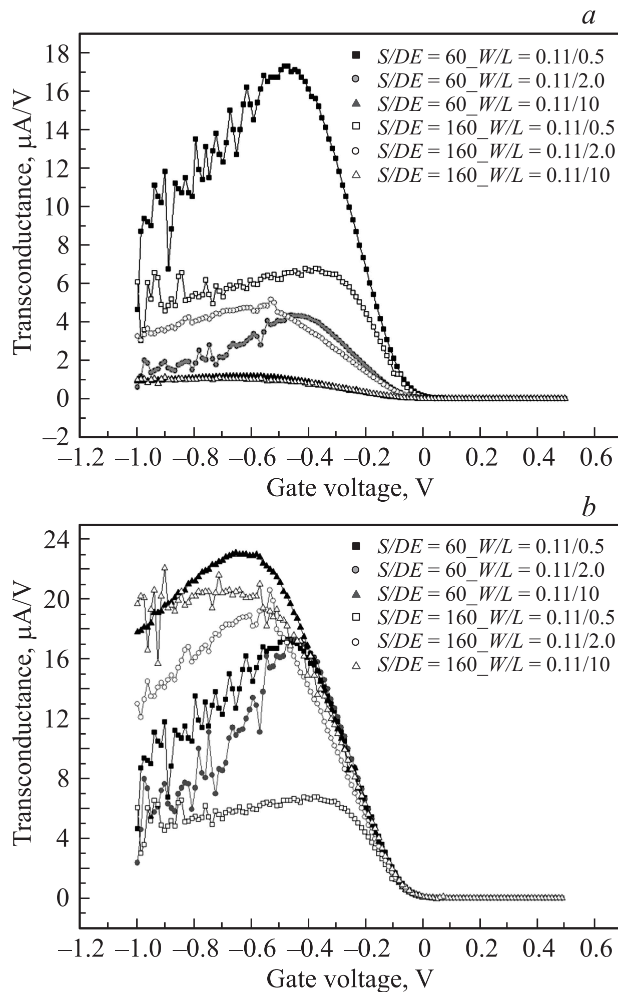

Figure 4. G_m vs. gate voltage characteristics: a — original measurement data and b — normalized data with the view of the identical *poly*-Si gate channel length, $L_{\text{G}} = 0.5\,\mu$m.

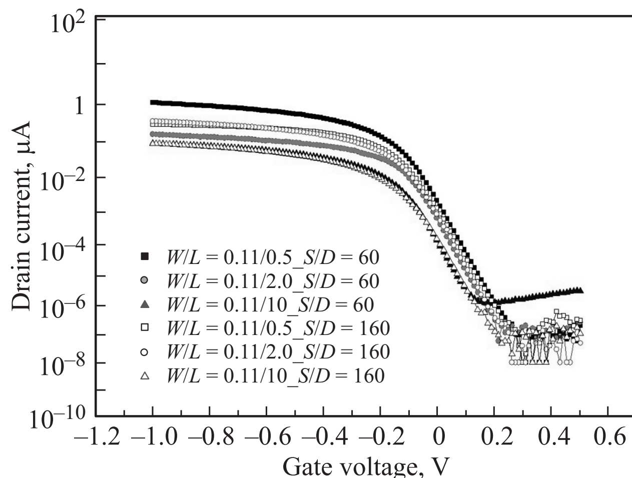

Figure 5. I_{D} vs. V_{G} curves for the various *poly*-Si gate channel lengths at $V_{\text{D}} = -0.05$ V as $W_{\text{fin}} = 0.11\,\mu$m.

channel resistance R_T including the p^+ resistance at the source region R_S, S/D ext. implant region R_{SDE}, channel resistance at the device ON state R_{CH}, R_{SDE} close to the drain zone, and p^+ resistance at the drain region R_{D} if the contact resistance is temporarily ignored. According to the references [1,23], we gain the S/D current IDS at the linear region expressed as

$$I_{\text{DS}} = \frac{W_{\text{eff}}}{L_{\text{eff}}}\mu_n C_{\text{ox}}\left(V_{\text{GS}} - V_T - \frac{1}{2}V_{\text{DS}}\right)V_{\text{DS}}, \qquad (2)$$

where L_{eff} — effective channel length $= L_g - \Delta L$, ΔL — channel length reduction, W_{eff} — effective channel length $= W_g - \Delta W$, and ΔW — channel length reduction.

Because we concern the S/D ext. resistance influences the S/D current, this factor must be included in consideration. First of all, the W_{eff} is fixed as the same size in all tests. The R_T value can be represented as

$$\frac{V_{\text{DS}}}{I_{\text{DS}}} = R_T = R_{\text{CH}} + R_{\text{D}} + R_{\text{S}} + 2R_{\text{SDE}}$$

$$= \frac{L_g - \Delta L}{W_{\text{eff}}}\frac{1}{\mu_n C_{\text{ox}}\left(V_{\text{GS}} - V_T - \frac{1}{2}V_{\text{DS}}\right)} + R_{\text{D}} + R_{\text{S}} + 2R_{\text{SDE}}. \qquad (3)$$

Assuming the S/D series resistance $R_{\text{P}} = R_{\text{S}} + R_{\text{D}} + 2R_{\text{SDE}}$, the Eq. (3) can be simplified as

$$\frac{V_{\text{DS}}}{I_{\text{DS}}} = R_{\text{CH}} + R_{\text{P}}$$

$$= \frac{L_g - \Delta L}{W_{\text{eff}}}\frac{1}{\mu_n C_{\text{ox}}\left(V_{\text{GS}} - V_T - \frac{1}{2}V_{\text{DS}}\right)} + R_{\text{P}}. \qquad (4)$$

In measurement of p-channel FinFETs (pFinFETs), $(V_{\text{GS}} - V_T - 1/2V_{\text{DS}})$ is changed from -0.05 V to -0.15 V with step -0.05 V as $V_{\text{DS}} = -0.05$ V fixed, as shown in Figs 6 and 7 represented for $L_{\text{SDE}} = 60$ and 160 nm, respectively. The channel width was fixed, but the channel lengths were different. The extracted R_p and ΔL values for 60 and 160 nm L_{SDE} are represented at Table 1. There are two intercepts in the subsets of Figs 6 and 7. Comparing the first intercept point between $V_{\text{GS}} - V_T = -0.05$ V and -0.1 V and the second one between $V_{\text{GS}} - V_T = -0.05$ V and -0.15 V, we observe that the $|V_{\text{GS}} - V_T|$ increases and the intercept point moves down to the lower due to the possible mechanism of mobility degradation [23]. In Table 1, the R_P resistance at $L_{\text{SDE}} = 160$ nm is greater than that at $L_{\text{SDE}} = 60$ nm, larger than the ratio of $R_{\text{SDE_160}}$ and $R_{\text{SDE_60}}$ which means the S/D ext. implant in diffusion or non-uniformity effect of surface channel for $L_{\text{SDE}} = 160$ nm is more obvious and increases the ΔL value. In the extraction of R_{SD} and R_{SDE}, we can't simply assume $R_{\text{SDE_60}}/R_{\text{SDE_160}} = 60/160$ to gain the previous both results because the boron diffusion effect after S/D ext. implant must be considered, especially with simulation assistance.

Continuously, when the LSDE is shortened from 160 to 60 nm, the drive current (I_{DS}) at the same W/L device is greater than that with the longer one, as

Table 1. Extracted I_{DS} data with original state and normalization: a — $V_{GS} - V_T = -1$ V and $V_{DS} = -1$ V; b — $V_{GS} - V_T = -1$ V and $V_{DS} = -2$ V

(*a*)

	0.5_S/DE = 60	2_S/DE = 60	10_S/DE = 60	0.5_S/DE = 160	2_S/DE = 160	10_S/DE = 160
Original data	19.8	4.7	1.27	15.3	5.37	1.38
Normalization	19.8	18.8	25.4	15.3	21.5	27.5

(*b*)

	0.5_S/DE = 60	2_S/DE = 60	10_S/DE = 60	0.5_S/DE = 160	2_S/DE = 160	10_S/DE = 160
Original data	23.8	6.41	1.30	20.0	5.61	1.40
Normalization	23.8	25.6	26.1	20.0	22.4	27.9

Table 2. Summarization of R_P and ΔL at the first intercept point between $V_{GS} - V_T = -0.05$ V and -0.1 V and the second one between $V_{GS} - V_T = -0.05$ V and -0.15 V

(*a*)

	0.5_S/DE = 60	2_S/DE = 60	10_S/DE = 60	0.5_S/DE = 160	2_S/DE = 160	10_S/DE = 160
Original data	19.8	4.7	1.27	15.3	5.37	1.38
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(*b*)

	0.5_S/DE = 60	2_S/DE = 60	10_S/DE = 60	0.5_S/DE = 160	2_S/DE = 160	10_S/DE = 160
Original data	23.8	6.41	1.30	20.0	5.61	1.40
Normalization	23.8	25.6	26.1	20.0	22.4	27.9

shown in Fig. 3, a, no matter what the W/L is in this tested comparison. However, if the tested devices are normalized with the identical channel length as shown in Fig. 3, b, the highest current at $V_D = -2$ V entering the saturation mode is located at the $W/L = 0.11/10$ (μm/μm)

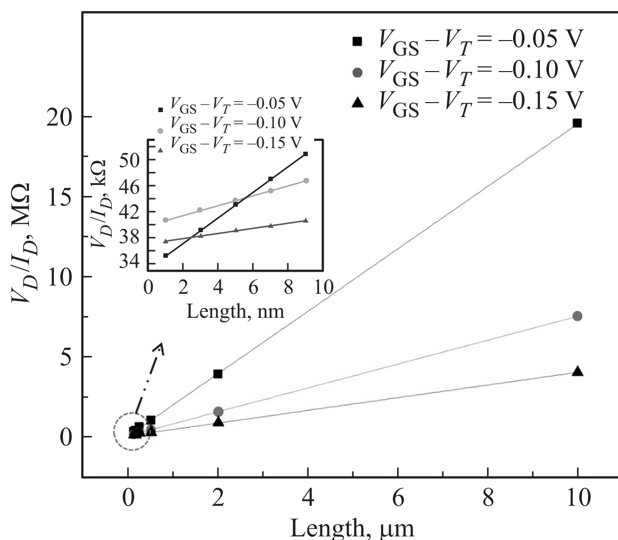

Figure 6. Determination of R_P series resistance and ΔL in pFinFETs as $V_{DS} = -0.05$ V fixed and $L_{SDE} = 60$ nm, but ($V_{GS} - V_T$) varies. The intercept points in subset are demonstrated.

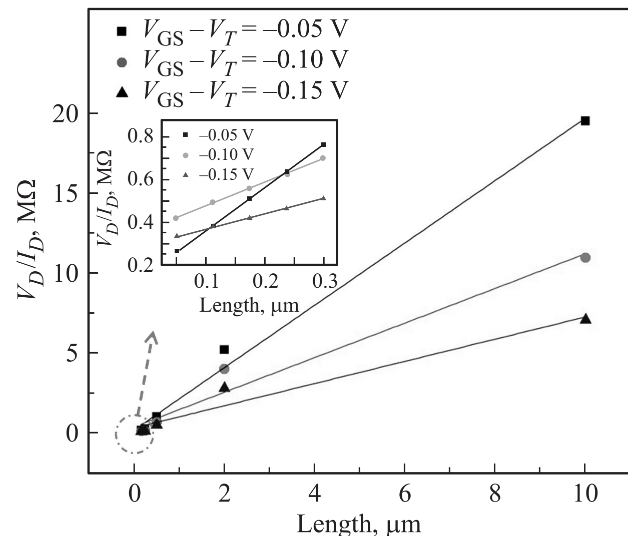

Figure 7. S/D R_P and ΔL in pFinFETs as $V_{DS} = -0.05$ V fixed and $L_{SDE} = 160$ nm. The subset illustrates the intercept phenomenon.

with $L_{SDE} = 160$ nm, as shown in Table 2. Using the normalization methodology, the drain current at channel length $L_G = 0.5\,\mu$m is the main index and the others aimed at that are multiplied by 4 or 20 times, respectively. Due to the suppressed contribution of R_{SDE} in normalization, the

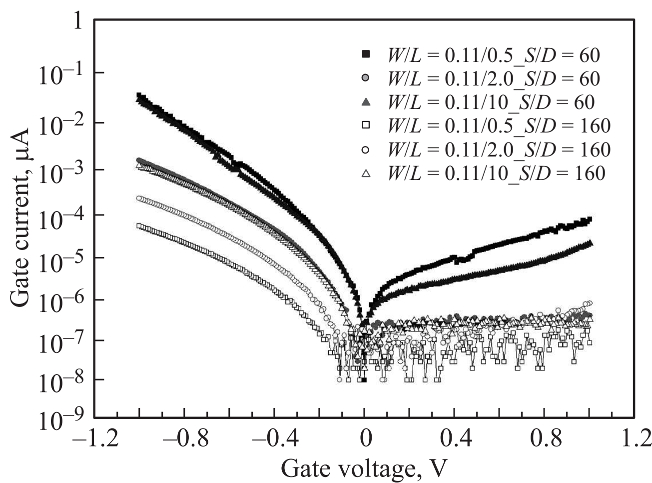

Figure 8. Gate leakage for the tested *p*FinFETs as $V_D = V_S =$ GND.

device for $W/L = 0.11/10$ (μm/μm) with $L_{SDE} = 160$ nm is slightly higher than that for $W/L = 0.11/05$ (μm/μm) with $L_{SDE} = 60$ nm. Generally, the shorter L_{SDE} provides compacter choice in IC design, but the leakage at G/D or G/S terminals is slightly increased, as shown in Fig. 8. Thus, the compromise between IC area density and device leakage increasing the OFF current must be handled deliberately.

For the trans-conductance variables related to the channel mobility, the maximum G_m for the original extracted data is at the $W/L = 0.11/0.5$ (μm/μm) with $L_{SDE} = 60$ nm, as shown in Fig. 4, *a*. Nevertheless, if we do the same normalization metrology following the drain current-like, the maximum G_m is changed to the $W/L = 0.11/10$ (μm/μm) with $L_{SDE} = 60$ nm, as shown in Fig. 4, *b*. The subthreshold swing (SS) value, as shown in Table 3, exhibits the maximum value located at $W/L = 0.11/10$ (μm/μm) with $L_{SDE} = 160$ nm.

Table 3. The measured subthreshold swing (mV/decade) values of the tested *p*FinFETs with varied L/L_{SDE} (μm/nm) and $W = 0.11$ (μm) fixed

L/L_{SDE} (μm/nm)	0.5/60	2/60	10/60	0.5/160	2/160	10/160
SS (mV/dec)	66.1	62.1	61.9	70.9	71.7	75.7

4. Conclusions

In this work, the longer L_{SDE} provides the better isolation between the S/D contact and the gate electrode. But the drive current will be suffered due to higher series S/D ext. resistance. In extraction of R_{SD} and R_{SDE}, the assumption can?t be simplified with $R_{SDE_160}/R_{SDE_60} = 160/60$ due the boron diffusion effect after the S/D ext. implant. For the shorter L_{SDE}, the device performance in ON current is better than that with the longer one. However, the OFF current in isolation capability for longer LSDE is more impressive than the shorter one. Of course, if the etch process can't be controlled well, these benefits will be discounted. Through this analysis, the S/D extension length contributing to the FinFET device performance [24–26] can be sensed well. This helpful information in FinFET fabrication offers the manufacturing team in decision of chosen OFF or ON current in the need of different HPC IC products.

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