Comparative investigation of GaAsSb/InGaAs type-II and InP/InGaAs type-I doped–channel field–effect transistors

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DC performance of GaAsSb/InGaAs type-II and InP/InGaAs type-I doped−channel field−effect transistors (DCFETs) is demonstrated and compared by two-dimensional simulated analysis. As compared with the traditional InP/InGaAs DCFET, the GaAsSb/InGaAs DCFET exhibits a higher drain current of 8.05 mA, a higher transconductance of 216.24 mS/mm, and a lower gate turn-on voltage of 0.25 V for the presence of a relatively large conduction band discontinuity ($\Delta E_c \approx 0.4$ eV) at GaAsSb/InGaAs heterostructure and the formation of two-dimensional electron gas in the n^+-InGaAs doping channel. However, due to the tunneling effect under large gate-to-source bias, it results in considerably large gate leakage current in the GaAsSb/InGaAs DCFET.

1. Introduction

Over the past years, InP/InGaAs heterostructure field-effect transistors (HFETs) have been considered to be the promising devices in microwave and optoelectronic integrated circuits because of the high electron mobility, large peak saturation velocity in the InGaAs channel layer, and good selective etching between InP and InGaAs materials [1–3]. Among of the HFETs, the transconductance values of high electron mobility transistors (HEMTs) might be relatively high due to the two-dimensional electron gas (2DEG) in the modulated channel, however, they suffered from poor device linearity and low output current [4]. In order to improve the device linearity and reduce the higher order harmonic terms in linear amplifiers, an alterable HFET, i. e., doping-channel FET (DCFET), was investigated to exhibit broad gate voltage swing [5,6]. For the DCFET, a large energy-gap undoped (or low-doped) material layer was employed as gate Schottky barrier layer to increase the gate turn-on voltage and enhance the drain current [5]. With respect to the InP/$In_{0.53}Ga_{0.47}As$ type-I heterojunction material system, the DCFETs with a conduction band discontinuity ($\Delta E_c \approx 0.23$ eV) value at the heterojunction can provide good carrier confinement effect in channel to achieve high gate forward bias, high drain output current, and broad gate voltage swing, simultaneously [6]. Recently, InP/GaAsSb type-II material system has been a new alternative for InP-based double heterojunction bipolar transistors (DHBTs) [7,8]. In the structures, the current blocking effect could be completely eliminated attributed that the conduction band edge of GaAsSb base layer lies above that of the InP emitter layer.

In this paper, a new GaAsSb/InGaAs DCFET constructed on InP substrate is first demonstrated. As compared with the conventional InP/InGaAs type-I DCFET, the GaAsSb/InGaAs type-II DCFET with a large ΔE_c value shows a larger transconductance value and a higher drain current. The device mechanism of GaAsSb/InGaAs and InP/InGaAs DCFETs will be demonstrated and compared in detail.

2. Device structures

The device structure of the studied GaAsSb/InGaAs DCFET (labeled device A) includes a 2000 Å undoped InP buffer layer, a 100 Å $n^+ = 1 \cdot 10^{18}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ channel layer, a 200 Å undoped $GaAs_{0.51}Sb_{0.49}$ gate layer and a 300 Å $n^+ = 1 \cdot 10^{19}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ cap layer. For comparison, another InP/InGaAs DCFET (labeled device B) has the similar structure as the device A except that a 200 Å undoped InP gate layer is employed to replace the GaAsSb layer. A two-dimensional (2D) semiconductor simulation package SILVACO was used to analyze the energy band, distributions of electrons, and dc performance of the two devices [9]. The 2D analysis takes into account the Poisson equation, continuity equation of electrons, Shockley-Read-Hall (SRH) recombination, Boltzmann statistics, and Fermi-Dirac statistics, simultaneously. The gate dimension and spacer of the drain-to-source were $1 \cdot 70\,\mu m^2$ and $3\,\mu$m, respectively.

3. Results and discussion

The energy bands of the devices A and B before the junction is formed are illustrated in Fig. 1. The electron affinities (energy gaps) of $GaAs_{0.51}Sb_{0.49}$, $In_{0.53}Ga_{0.47}As$, and InP materials are of 4.23 (0.68), 4.63 (0.75), and 4.4 (1.35) eV, respectively [10,11]. Apparently, the $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$ and InP/$In_{0.53}Ga_{0.47}As$ heterojunctions form the type-II and type-I heterostructures, respectively. Furthermore, the ΔE_c value at $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$ heterojunction is estimated to be 0.4 eV, which is higher than that of 0.23 eV at InP/$In_{0.53}Ga_{0.47}As$ heterojunction. The corresponding energy band diagrams at equilibrium and at gate-to-source

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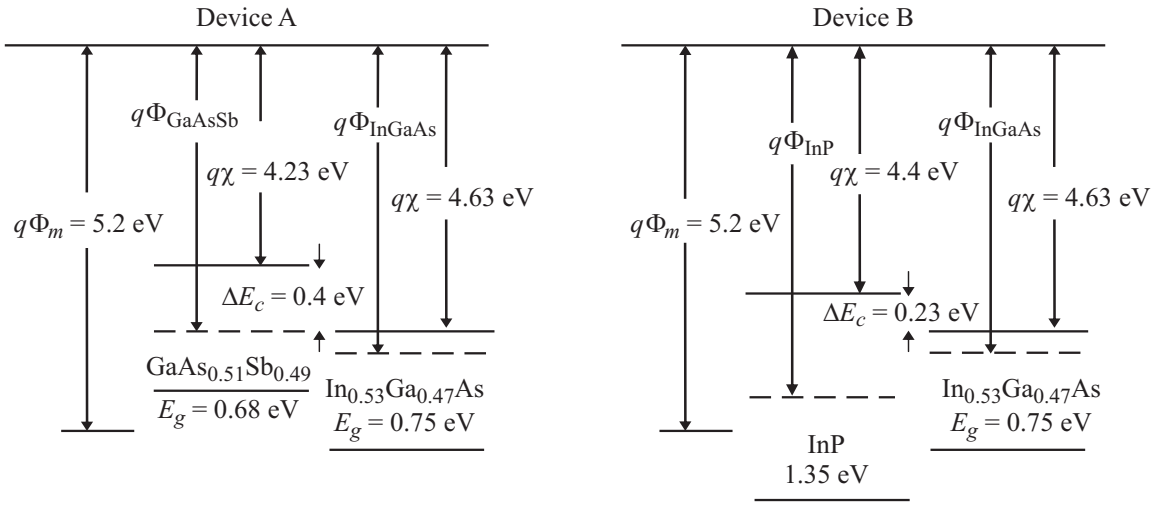

Рис. 1. Schematic energy bands of the devices A and B before the junction is formed. The devices A and B represent the GaAsSb/InGaAs and InP/InGaAs doping-channel FETs, respectively.

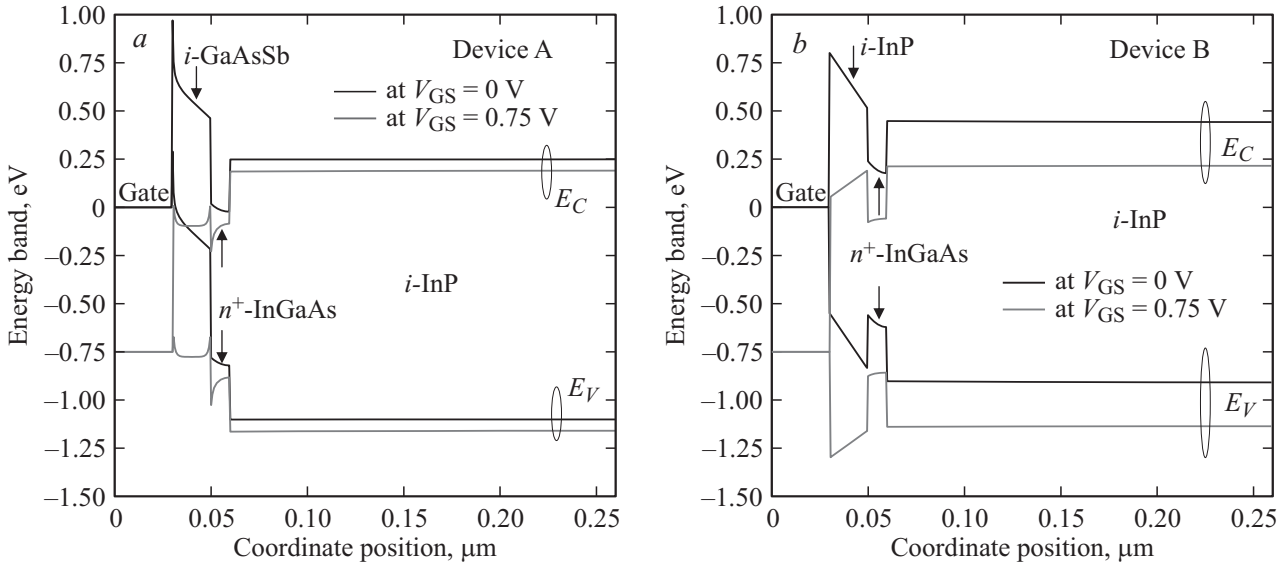

Рис. 2. Corresponding energy band diagrams of the (*a*) device A and (*b*) device B at equilibrium at $V_{GS} = 0.75$ V.

forward voltage of +0.75 V for the devices A and B are depicted in Figs. 2, *a* and *b*, respectively. When compared with the device B, for the considerable work function difference ($q\Phi_m \gg q\Phi_{GaAsSb}$) between Au metal and $GaAs_{0.51}Sb_{0.49}$ layer, it will form a relatively large potential spike at the metal-semiconductor junction in the device A. It is worthy to note that at thermal equilibrium the conduction band of the n^+-$In_{0.53}Ga_{0.47}As$ channel is lower than the Fermi level because the conduction band discontinuity ($\Delta E_c \sim 0.4$ eV) at $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$ heterojunction is enough large. Therefore, 2DEG will be formed in the n^+-$In_{0.53}Ga_{0.47}As$ quantum-well channel and the device A will act as a depletion-mode transistor. However, because the ΔE_c value is only 0.23 eV at $InP/In_{0.53}Ga_{0.47}As$ heterojunction in the device B, the n^+-$In_{0.53}Ga_{0.47}As$ channel is completely depleted at equilibrium and it behaviors as an enhancement-mode transistor. Significantly, another large as well as thin potential spike at i-$GaAs_{0.51}Sb_{0.49}/n^+$-$In_{0.53}Ga_{0.47}As$ heterojunction apparent under large gate forward bias in the device A, while there is not any potential spike formed in the i-InP gate layer in the device B.

Fig. 3, *a* and *b* illustrate the electron distribution at equilibrium and under forward bias for the device A and B, respectively. Clearly, a considerably high electron concentration above 10^{20} cm^{-3} at $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$ heterojunction is observed in the device A. Nevertheless, the device B shows lower

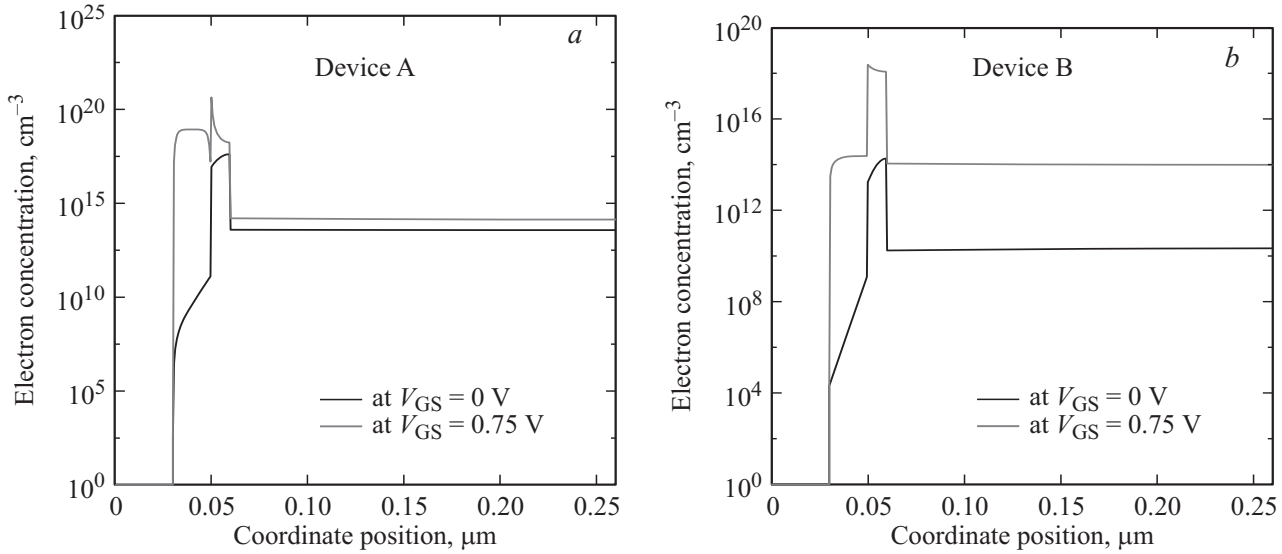

Рис. 3. Electron concentrations of the (a) device A and (b) device B at equilibrium at $V_{GS} = 0.75$ V.

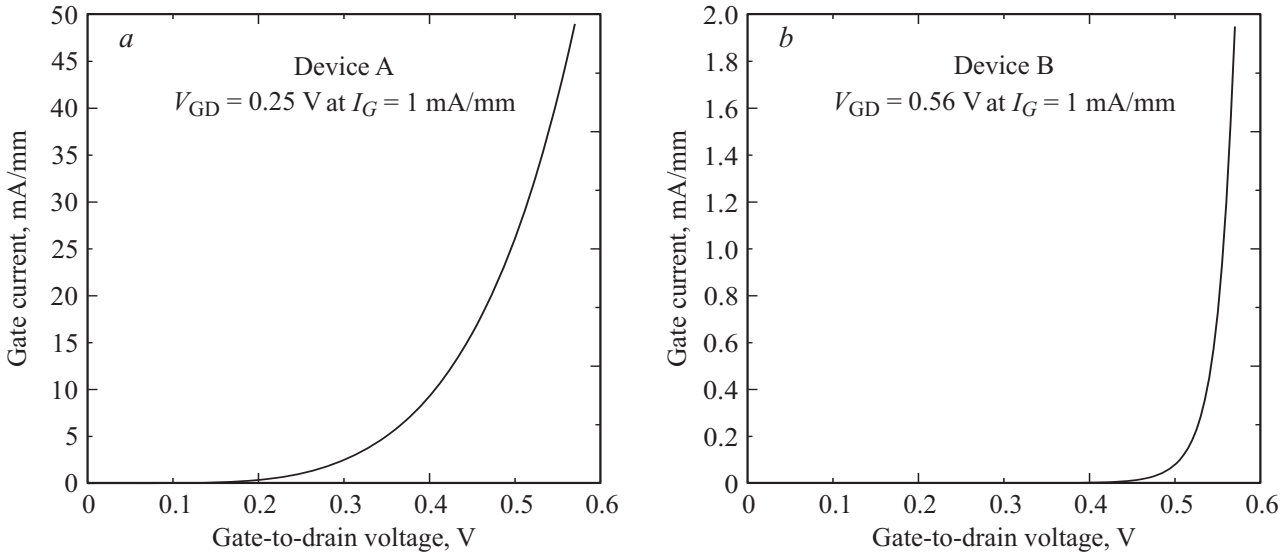

Рис. 4. Gate-to-drain forward current-voltage characteristics of the (a) device A and (b) device B.

electron concentration than the device A because of the smaller ΔE_c value at InP/$In_{0.53}Ga_{0.47}As$ jeterojunction. The gate-to-source forward current-voltage $(I\text{-}V)$ characteristics of the devices A and B are shown in Fig. 4, *a* and *b*, respectively. At gate current of 1 mA/mm, the gate-to-source forward turn-on voltages are of 0.25 and 0.56 V for the devices A and B, respectively. As seen in Fig. 2, *a*, part of electrons in the InGaAs channel could transport into gate electrode through the double potential spikes by tunneling behavior under forward gate bias. Therefore, the device A exhibits a smaller turn-on voltage than the device B.

The simulated common-source *I-V* characteristics of the devices A and B are revealed in Figs 5, *a* and *b*, respectively. In the device A (device B), the gate voltages are operated from -0.1 $(+0.1)$ V to $+1.0$ $(+2.0)$ V and a maximum drain saturation current of 8.05 (6.84) mA is observed. In the device A, the 2DEG formed in the InGaAs channel may be increased and modulated with the gate bias due to the large ΔE_c value at $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$ heterojunction. This will substantially increase drain current. Nevertheless, considerably large gate leakage currents are observed in the device A. This phenomenon can be attributed to the carrier tunneling behavior as the above description. Figs 6, *a* and *b* illustrate the transconductance and drain saturation current versus the gate-to-source voltage for the devices A and B, respectively. The threshold voltage V_{th} is of -0.1 $(+0.1)$ V in the device A (device B). A maximum transconductance as high as

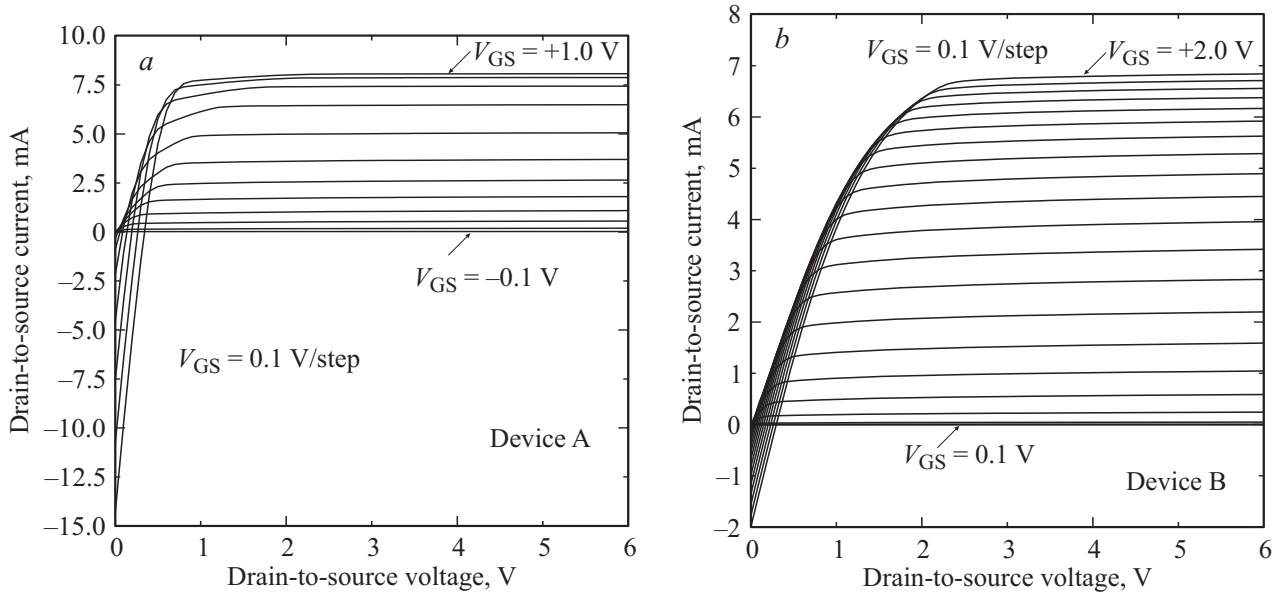

Рис. 5. Common-source current-voltage characteristics of the (*a*) device A and (*b*) device B.

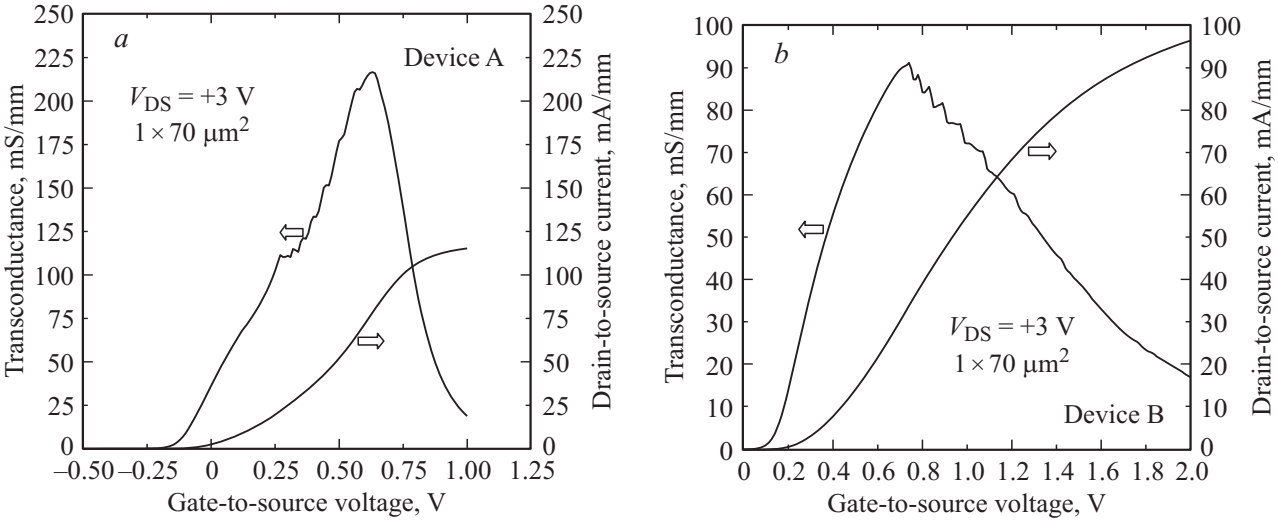

Рис. 6. Transconductance and drain saturation current versus gate-to-source voltage of the (*a*) device A and (*b*) device B.

216.2 (91.14) mS/mm and a maximum drain current of 115.02 (96.8) mA/mm at $V_{DS} = +3$ V are obtained. For comparison, the device A exhibits a larger transconductance than the device B for the larger drain current resulting from the 2DEG formation in the n^+-InGaAs channel when the gate-to-source voltage is biased from threshold voltage to +1 V.

4. Conclusion

A newly designed $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$ DCFET is investigated by two-dimensional analysis. As compared to the $InP/In_{0.53}Ga_{0.47}As$ type-I DCFET, the proposed $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$ type-II DCFET exhibits higher transconductance, higher drain output current, and lower gate turn-on voltage for the formation of 2DEG in the n^+-InGaAs channel. However, apparent gate leakage current is observed in the $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$ DCFET. The phenomenon can be attributed to the tunneling behavior for presence of two potential spikes at metal/i-$GaAs_{0.51}Sb_{0.49}$ and i-$GaAs_{0.51}Sb_{0.49}/n^+$-$In_{0.53}Ga_{0.47}As$ heterojunctions under large gate forward bias. Consequently, the studied GaAsSb/InGaAs type-II DCFET shows better DC characteristics than the traditional $InP/In_{0.53}Ga_{0.47}As$ type-I DCFET except the gate leakage current.

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