Comparative investigation of InP/InGaAs heterostructure-emitter tunneling and superlattice bipolar transistors

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In this article, the characteristics of InP/InGaAs heterostructure-emitter bipolar transistors with 30 Å, 50 Å *n*-InP layer tunneling layers and a five-period InP/InGaAs superlattice are demonstrated and comparatively investigated by experimentally results and analysis. In the three devices, a 200 Å *n*-$In_{0.53}Ga_{0.47}As$ layer together with an *n*-InP tunneling emitter layer (or *n*-InP/*n*-InGaAs superlattice) forms heterostructure emitter to decrease collector-emitter offset voltage. The results exhibits that the largest collector current and current gain are obtained for the tunneling transistor with a 30 Å *n*-InP tunneling emitter layer. On the other hand, some of holes injecting from base to emitter will be blocked at *n*-InP/*n*-InGaAs heterojunction due to the relatively small hole transmission coefficient in superlattice device, which will result in a considerable base recombination current in the *n*-InGaAs layer. Therefore, the collector current and current gain of the superlattice device are the smallest values among of the devices.

1. INTRODUCTION

The InP/InGaAs heterojunction bipolar transistors (HBTs) are emerging as key devices for high-speed electronic and optoelectronic applications [1–3]. They provide several advantages than the GaAs-based HBTs attributed to the excellent properties, such as

(I) low electron mass in InGaAs material,

(II) high etching selectivity between InP and InGaAs layers,

(III) low surface recombination velocity of InGaAs base layer,

(IV) a small base-emitter (B-E) turn-on voltage, and

(V) compatibility with long wavelength photonic devices. As to the InP/InGaAs HBTs, high emitter injection efficiency and current gain were achieved for the large valence band discontinuity (ΔE_v) of 0.35 eV at InP/InGaAs heterojunction [4–6]. However, a considerable conduction band discontinuity (ΔE_c) of 0.25 eV at the heterojunction still is an significant factor to cause a large collector-emitter (C-E) offset voltage (ΔV_{CE}), which will substantially increase unnecessary power consumption in low power circuit applications [7,8]. Previously, some improved structures, such as delta-doped and double heterjunction HBTs, etc., had been well studied to reduce the offset voltage [9,10]. Nevertheless, the doping level must be accurately controlled in the delta-doped HBT [9]. In the double heterjunction HBTs, the existance of knee curves in current–voltage (I–V) characteristics, resulting from the electron blocking effect at abrupt base-collector heterojunction, will enable the collector current and current gain to reduce considerably [10].

Furthermore, the quantized devices with carrier tunneling behavior have attracted significant interest for high-speed conduction and multifunction application [11–13]. Among of the quantized devices, HBTs employ a thin tunneling barrier in place of a wide energy-gap emitter, i.e. so-called tunneling-emitter bipolar transistors (TEBTs), have been applied in signal amplifiers and high-speed microwave circuits [11,12]. The tunneling emitter acts as an effective mass filter between electrons and holes to provide good confinement effect for holes and short transporting path across the emitter region for electrons, simultaneously. Similarly, superlattice-emitter bipolar transistors (SEBTs) could also maintain good hole confinement effect and reduce non-radiative recombination cross-section by the resonant tunneling injection [13]. In this article, the characteristics of InP/InGaAs heterostructure-emitter tunneling and superlattice bipolar transistors will be comparatively investigated. The influence of tunneling layer thickness on the heterostructure-emitter tunneling bipolar transistors are also discussed in the text.

2. Experiments

The studied InP/InGaAs heterostructure–emitter tunneling bipolar transistors and superlattice bipolar transistor were grown on by low-pressure metal–organic chemical–vapor deposition system (LP-MOCVD) an (100) oriented semi-insulating InP substrate. The epitaxial layers of the heterostructure-emitter tunneling bipolar transistors consisted of a 0.5 μm $n^+ = 10^{19}\,\mathrm{cm}^{-3}$ $In_{0.53}Ga_{0.47}As$ sub-collector layer, a 0.5 μm $n^- = 2 \cdot 10^{16}\,\mathrm{cm}^{-3}$ $In_{0.53}Ga_{0.47}As$ collector layer, a 0.1 μm $p^+ = 10^{19}\,\mathrm{cm}^{-3}$ $In_{0.53}Ga_{0.47}As$ base layer, a 200 Å $n = 5 \cdot 10^{17}\,\mathrm{cm}^{-3}$ small energy-gap $In_{0.53}Ga_{0.47}As$ layer, a $n = 5 \cdot 10^{17}\,\mathrm{cm}^{-3}$ InP tunneling emitter layer. Finally, a 0.2 μ $n^+ = 10^{19}\,\mathrm{cm}^{-3}$ $In_{0.53}Ga_{0.47}As$ cap layer was deposited on the tunneling emitter layer. Two device structures with 30 and 50 Å InP tunneling emitter layer are labeled devices A and B, respectively. In addition, the third device, i.e., InP/InGaAs heterostructure-

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The epitaxial layers of the studied devices

Layer	Device *A*	Device *B*	Device *C*
Cap	n^+-$In_{0.53}Ga_{0.47}As$ (0.2 μm)	n^+-$In_{0.53}Ga_{0.47}As$ (0.2 μm)	n^+-$In_{0.53}Ga_{0.47}As$ (0.2 μm)
Emitter	*n*-InP (30 Å)	*n*-InP (50 Å)	n – InP (50 Å) n – $In_{0.53}Ga_{0.47}As$ (50 Å) . . n – $In_{0.53}Ga_{0.47}As$ (50 Å) n – InP (50 Å)
Small energy-gap layer	*n*-$In_{0.53}Ga_{0.47}As$ (200 Å)	*n*-$In_{0.53}Ga_{0.47}As$ (200 Å)	*n*-$In_{0.53}Ga_{0.47}As$ (200 Å)
Base	p^+-$In_{0.53}Ga_{0.47}As$ (0.1 μm)	p^+-$In_{0.53}Ga_{0.47}As$ (0.1 μm)	p^+-$In_{0.53}Ga_{0.47}As$ (0.1 μm)
Collector	n^--$In_{0.53}Ga_{0.47}As$ (0.5 μm)	n^--$In_{0.53}Ga_{0.47}As$ (0.5 μm)	n^--$In_{0.53}Ga_{0.47}As$ (0.5 μm)
Subcollector	n^+-$In_{0.53}Ga_{0.47}As$ (0.5 μm)	n^+-$In_{0.53}Ga_{0.47}As$ (0.5 μm)	n^+-$In_{0.53}Ga_{0.47}As$ (0.5 μm)
Substrate	S.I. InP	S.I. InP	S.I. InP

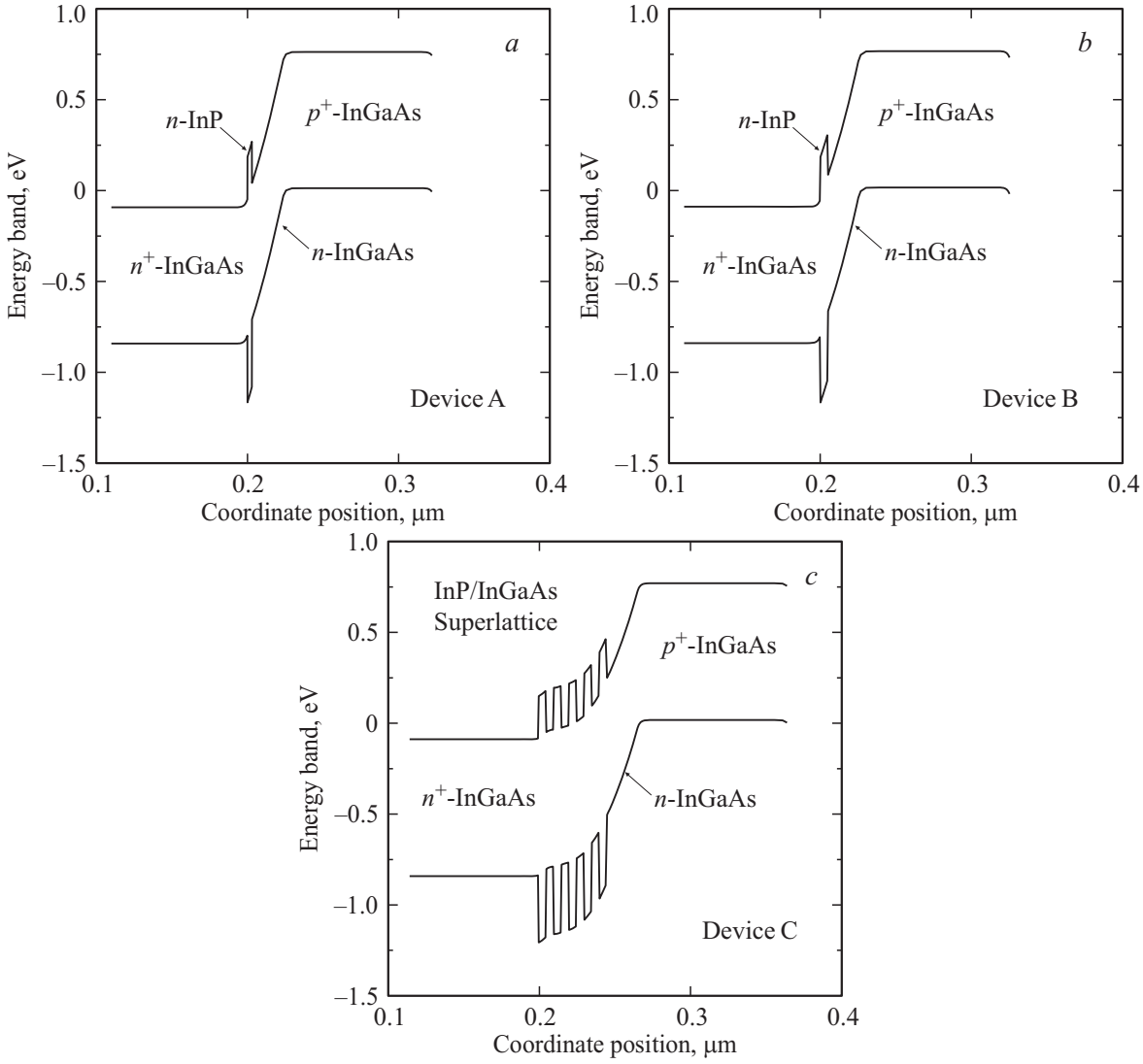

Figure 1. Corresponding energy-band diagrams at equilibrium of (*a*) device *A* with a 30 Å InP tunneling layer, (*b*) device *B* with a 50 Å InP tunneling layer, and (*c*) device *C* with InP/InGaAs superlattice.

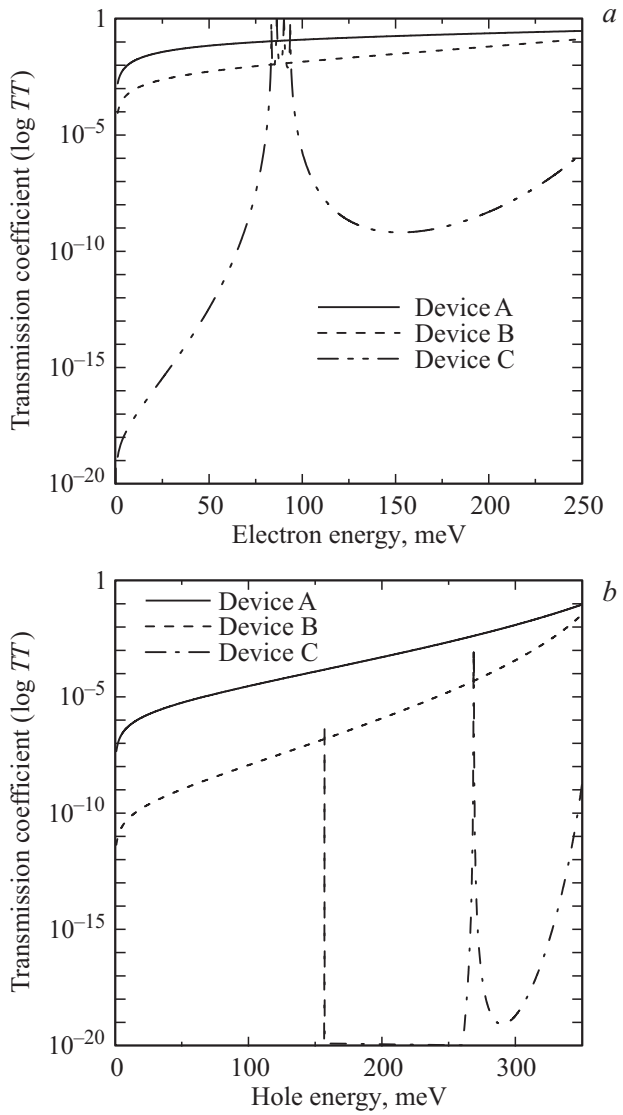

Figure 2. Relationships of transmission coefficients versus (*a*) electron energy and (*b*) hole energy under ideal flat-band condition.

emitter superlattice bipolar transistor (labeled device *C*), had the same concentration as the above devices except that an InP/InGaAs superlattice is constructed to replace the InP tunneling emitter layer. The superlattice consisted of a five-period 50 Å *n*-InP barrier layers and a four-period 50 Å *n*-$In_{0.53}Ga_{0.47}As$ well layers. Trimethylindium (TMI), trimethylgallium (TEG), phosphine (PH_3), and arsine (AsH_3) were used as the In, Ga, P, and As sources, respectively. The dopants used for *n* and *p* layers were silane (SiH_4) and dimethylzine (DMZ), respectively. After the epitaxial growth, the conventional photolithography, vacuum evaporation and wet etching processes were used to fabricate the devices. The InGaAs and InP layers were selectively etched by the solutions of

$$H_3PO_4 : H_2O_2 : H_2O = 6 : 3 : 100$$

and

$$HCl : H_2O = 1 : 1,$$

respectively. The process began with AuGeNi metal evaporation for emitter contact and then emitter self-aligned mesa was formed and etching to the base layer. After the deposition of AuZn base metal, the base mesa was defined and formed by etching the base and collectors. Then, AuGeNi metal was deposited on the subcollector layer. The above ohmic contacts were formed by sintering at 450°C for 30 s. Finally, the device mesa was formed to provide the device isolation. Table 1 shows the structure layers of the studied devices. The emitter and collector areas are 50×50 and $100 \times 100\,\mu m^2$, respectively.

3. Experimental results and discussion

By solving Poisson's equations, the corresponding energy-band diagrams at equilibrium of the devices *A*, *B*, and *C* are plotted in Fig. 1, *a*, *b* and *c*, respectively. Obviously, the potential spike at $B-E$ junction is completely eliminated for the addition of a 200 Å *n*-$In_{0.53}Ga_{0.47}As$ layer. Therefore, a low ΔV_{CE} value can be expectable. In the devices, a small energy-gap *n*-InGaAs layer together with an *n*-InP tunneling emitter layer (or *n*-InP/*n*-InGaAs superlattice) forms the heterostructure emitter. Under transistor operation mode, part of electrons injecting from n^+-InGaAs cap layer could tunnel through the thin tunneling emitter (or superlattice) layer and easily transport over the small energy-gap *n*-InGaAs layer into the base region. Excellent device characteristics could be achieved for the large ratio of electron-to-hole transmission probability across the thin tunneling and superlattice layers. In addition, as considering the tunneling mechanism, the relationship of transmission coefficient versus electron energy under ideal flat-band condition is depicted in Fig. 2, *a*. At electron energy of 250 meV, the continue transmission coefficient reaches $3.0 \cdot 10^{-1}$ and $1.5 \cdot 10^{-1}$ in the devices *A* and *B*, respectively. As to the device *C*, it appears one resonant-tunneling subband for electron energy, i. e., from 83.5 to 90.2 meV, as seen in Fig. 2, *a*. On the other hand, the relationship of transmission coefficient versus hole energy is illustrated in Fig. 2, *b*. The continue transmission coefficients are of $8.2 \cdot 10^{-2}$ and $3.1 \cdot 10^{-2}$ at hole energy of 350 meV in the devices *A* and *B*, respectively. While, it appears two relatively narrow and weak subbands for hole energy in the device *C*. The transmission coefficients are of only $5.4 \cdot 10^{-7}$ and $7.3 \cdot 10^{-4}$ at hole energy of 157 and 268.8 meV, respectively.

Fig. 3, *a, b*, and *c* depict the typical common-emitter $I-V$ characteristics at room temperature of the devices *A*, *B*, and *C*, respectively. The device *A* exhibits a largest maximum collector current of 68.8 mA than that of 66.2 (52.1) mA in the device *B* (device *C*). Furthermore, low ΔV_{EC} values of about 60 mV are observed in the three devices. As the base-to-collector terminals are short, the Gummel plots of the devices *A*, *B*, and *C* are shown in Fig. 4, *a, b*, and

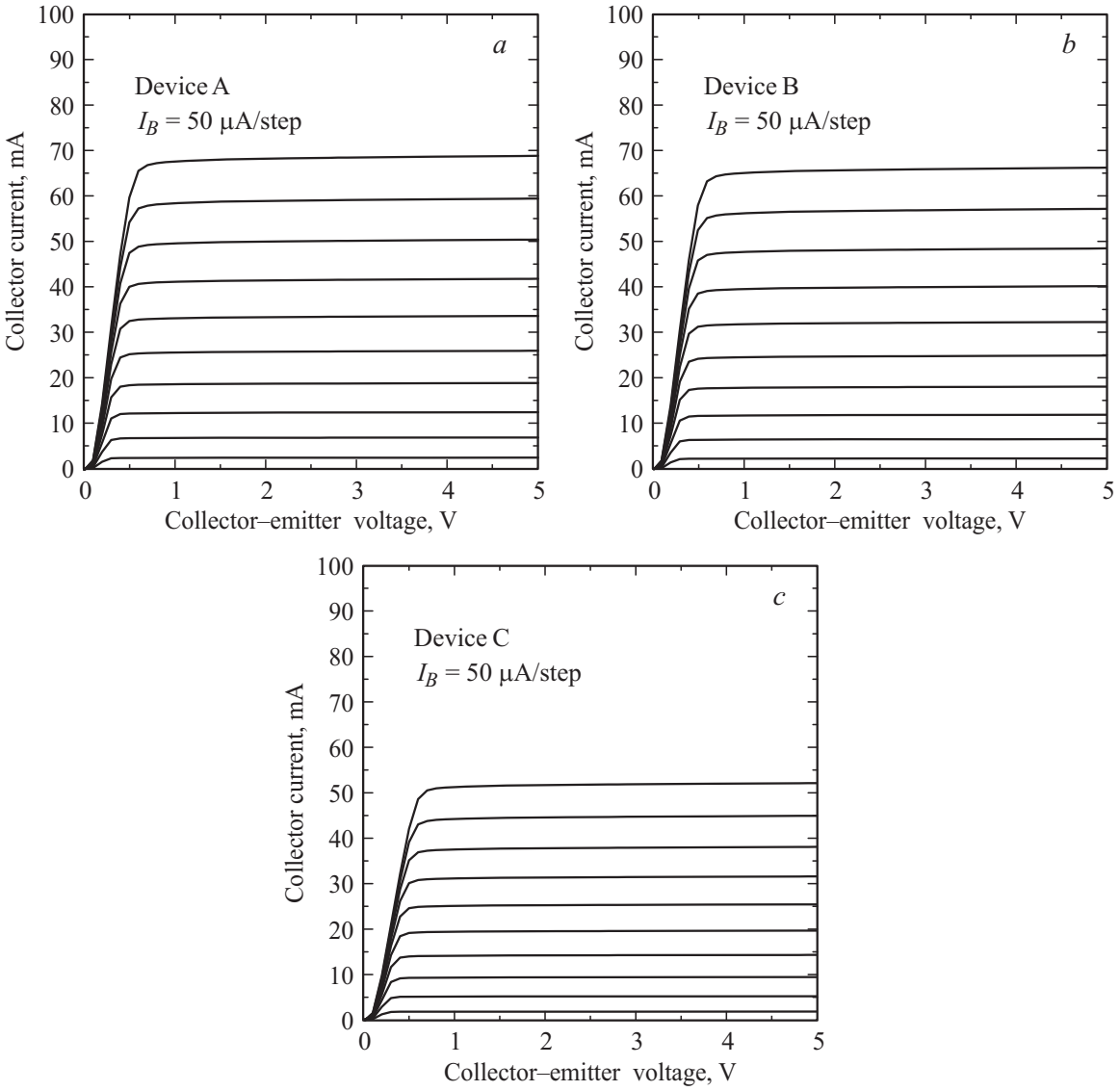

Figure 3. Typical common-emitter current-voltage characteristics at room temperature of (a) device A, (b) device B, and (c) device C.

c, respectively. The current gains of 137, 129, and 78 are obtained at $V_{BE} = 0.7$ V in the devices A, B and C, respectively. As current gain is equal to unity, the base-emitter voltages are of 0.345, 0.346, and 0.359 V for the devices A, B, and C, respectively. Mainly, the high current gains are due to the large ΔE_v value at InP/$In_{0.53}Ga_{0.47}As$ heterojunction to provide good confinement effect for holes, and the low ΔV_{EC} value could be attributed that the energy band at emitter side is reduced for effectively eliminating the potential spike at $B-E$ junction. At low current level, the ideality factors nc of collector currents are close to unity in the three devices. This denotes that the thermionic emission, tunneling, and diffusion mechanisms dominate the electron transportation across the $B-E$ junction. On the other hand, the ideality factors n_b of base currents at low current level are of 1.830, 1.837, and 1.914 in the devices A, B and C, respectively. Among of the devices, the device C exhibits the largest base recombination current. The performance comparison of the three devices is described as follows.

With respect to the tunneling HBTs, the device A shows larger slightly collector current and current gain at high current levels than the device B. That means that electrons will more easily tunnel across a thinner InP tunneling layer in the device A due to the higher transmission coefficient for electron energy. Though the device B has smaller transmission coefficients for hole energy, the slightly thicker InP tunneling layer could provide better confinement effect for holes at low $B-E$ bias than the device A. Accordingly, some of holes injecting from base to emitter will be blocked and accumulated at n-InP/InGaAs heterojunction in the device B, which could result in a slightly larger base recombination current in the small energy-gap n-GaAs emitter layer. Therefore, the base current is slightly increased and current gain is decreased when comparing

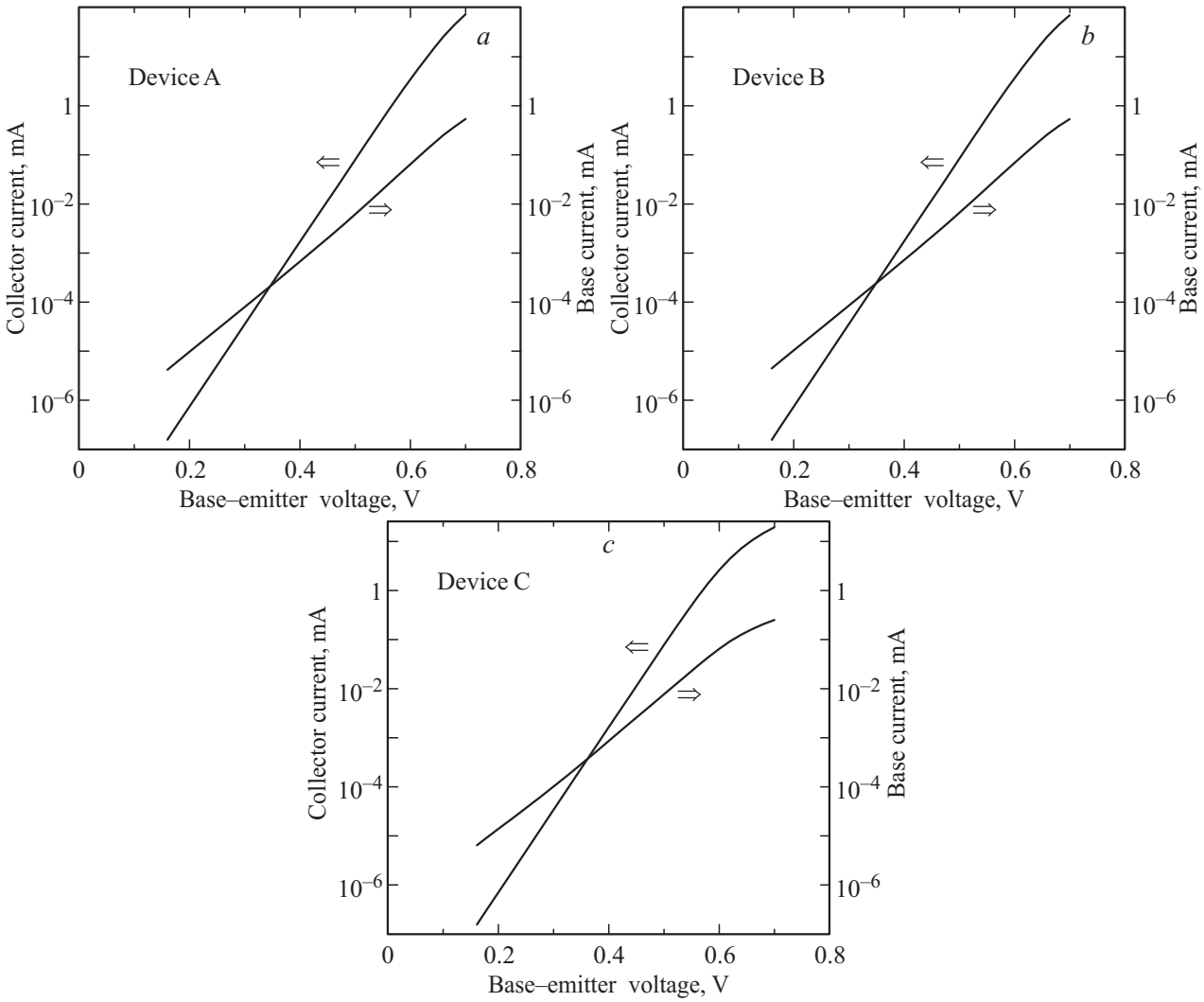

Figure 4. Gummel plots of (*a*) device *A*, (*b*) device *B*, and (*c*) device *C*.

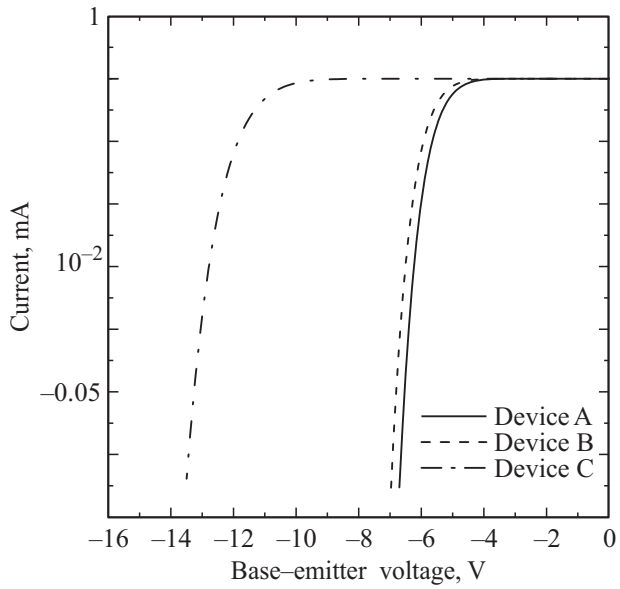

Figure 5. The current–voltage characteristics of the devices under base-emitter inverted biases at room temperature.

with the device *A*. On the other hand, the collector current of device *C* is smaller than the other devices because only some of electrons could enter the superlattice at somewhat electron energy by resonant tunneling behavior. Similarly, due to the relatively small transmission coefficients across the superlattice in the device *C*, more holes injecting from base to emitter will be accumulated in the small energy-gap *n*-InGaAs layer. Thus, a largest base current and a smallest current gain are observed in the device *C*.

Fig. 5 shows the $I-V$ characteristics of the devices under base-emitter inverted biases at room temperature. At current level of -10^{-5} Å, the base-emitter voltages are of -5.68, -5.98, and -11.85 V for the devices *A*, *B*, and *C*, respectively. The inverted voltage of device *C* is the largest because the total thickness of InP layers in the superlattice is the largest, while the device A has a smallest value for the thinnest InP tunneling layer.

4. Conclusion

We have successfully compared the characteristic difference of InP/InGaAs heterostructure-emitter bipolar transistors with tunneling and superlattice layersl. Attributed to the different carrier transmission behaviors across the tunneling- and superlattice layers, obvious variation in device characteristics are observed. The device mechanism including electron and hole transmission coefficient across tunneling layerand superlattice is also discussed. To compare with the superlattice device, the tunneling devices exhibit higher collector currents and current gains. In addition, the collector current and current gain of the device with 30 Å InP tunneling emitter are slightly larger than the device with 50 Å tunneling layer. Consequentially, the demonstration and comparison of the tunneling and superlattice transistors provide a promise for design in circuit applications.

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