Effect of post oxidation annealing on electrical characteristics of Ni/SiO_2/4H-SiC capacitor with varying oxide thickness

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This paper describes an experimental observation of post oxidation annealing (POA) treatment on current-voltage and capacitance-voltage characteristics of Ni/SiO_2/4H-SiC system with varying oxide thickness. The leakage current of fabricated structures shows an asymmetric behavior having noticeable effect of POA with the polarity of gate bias (+V or –V at the anode). When compared with the conventional wet oxidation, the POA processes greatly reduce interface-state density and enhance reliability of devices. An extensive increment in the barrier height at SiO_2/4H-SiC interface was observed due to POA, which resulted into lower forward leakage current. A significant improvement in the oxide charges are also demonstrated using $C-V$ characteristics of POA treated structures.

1. Introduction

The lack of high quality gate dielectrics has impeded the technology advancement in the field of SiC metal–oxide–semiconductor (MOS) devices [1]. SiC is a very attractive semiconductor material for high power, high frequency, high temperature and harsh environment applications because of its unique properties like wide bandgap (~ 3 eV), high thermal conductivity ($3.7-4.9\,\mathrm{W/(cm\cdot {}^\circ C)}$), high electron drift velocity ($2.0\cdot 10^7$ cm/s) and high breakdown field (3–5 MV/cm). An expected advantage of SiC over other compound semiconductors is its ability to grow SiO_2 layer that is readily formed in oxidizing ambient. However, it has been proven to be a difficult task to grow a high quality SiC/SiO_2 interface. This is, in particular, true for Si-face 4H-SiC, which is the most commonly used material for SiC device development.

In the fabrication of metal-oxide-silicon carbide (MOSiC) capacitor, a high surface state or so called near-interface trap were detected at the interface of SiO_2/4H-SiC with energy levels near the SiC conduction band edge [2–4]. These traps are believed to be located at some distance from the interface into the silicon dioxide and are responsible for the low inversion channel mobility in n-channel metal–oxide–semiconductor field effect transistors (MOSFETs) [5–7]. In case of silicon carbide material, the origin of the surface states is still unclear but recent observations suggest that silicon interstitial or carbon clusters are believed to the probable origins of surface states [8]. The quality of any oxide layer can be examined by the leakage current and oxide charges associated with the MOS system. Introduction of nitrogen at the interface is highly responsible for passivation of interface states. The density of interface states is significantly lower than in conventionally grown wet or dry oxides but their total density is not still satisfactory and electron trapping in interface states limits the field effect mobility in transistors.

In fact, many investigators have studied the possibility of incorporating the different annealing ambient into silicon dioxide by using several different techniques in the processing of Si-technology: (i) thermal oxidation of Si by N_2O and NF_3 gases [9], (ii) N_2O plasma treatment on PECVD-grown fluorinated silica glass (FSG) [10], (iii) NH_3-added PECVD-grown FSG [11], and (iv) fluorination and nitridation under microwave plasma for SiO_2 [12]. Similarly, in SiC-device technology number of techniques have also been introduced to enhance the quality of SiO_2 grown on SiC: viz (i) rapid thermal annealing [13], (ii) annealing in N_2O ambient [14], (iii) annealing in NO ambient [15], (iv) post metallization annealing [16] (v) SiO_2 grown by the method of sodium enhanced oxidation [17] and (vi) microwave annealing [18] and so on. All of these results showed positive trends with excellent dielectric properties after incorporating the different annealing ambient into the fabrication of SiO_2 films. Excluding all of these improvements, however, the incorporation of N by NH_3 would introduce a large concentration of electron traps in the films [19–21]. It is widely accepted that the presence of electron traps degrades device performance or characteristics. The incorporation of F would also lead to some oxide traps (i. e. Si dangling bonds) that increase the leakage current under moderate electric field [22]. The all above described methods were analyzed using a particular oxide thickness. In this paper, the oxide thickness was varied and significantly the effect was analyzed on $I-V$ and $C-V$ characteristics of MOSiC capacitor. On the other hand, to attain an improved process, it is our strong intention to incorporate the molecular nitrogen (N_2) at high temperature into silicon dioxide (SiO_2) to realize an oxide of remarkable quality with valuable characteristics.

In this reported work, molecular flow of N_2 with constant rates was used to reduce the leakage current and

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oxide charges. Wet thermal oxidation followed by thermal annealing in N_2 ambient was performed in quartz horizontal furnace. Experimental details of sample preparation, fabrication of MOSiC structures and electrical characterization methodology is given in the next section. Effect of POA on $I-V$ and $C-V$ characteristics are mentioned in the section thereafter, which is followed by conclusions.

2. Experimental details

A device grade n/n^+ type 4H-SiC substrate of $50\,\mu$m epitaxial layer on Si-face (nitrogen doped concentration; $9 \cdot 10^{14}\,\mathrm{cm}^{-3}$), 8° off axis (0001) oriented was used. The wafers were purched from CREE Research inc., USA. Prior to loading in a quartz furnace for the oxidation, Radio Corporation of America (RCA) chemical cleaning treatment was given to all samples. At once two samples were loaded for thermal oxidation at 800°C in nitrogen flow. Wet thermal oxidation was performed at 1110°C for fixed oxidation time. At this stage one sample was unloaded at 800°C in nitrogen flow. This sample was called „As processed sample". The remaining one sample was further loaded in to furnace for annealing in the flow of nitrogen. Annealing was performed at 1110°C for 30 min in the ambient of molecular nitrogen with constant flow rate and then sample was unloaded at 800°C. This sample was termed as „Annealed sample". This whole process of thermal oxidation and post oxidation annealing (POA) cycle was summarized in Fig. 1, *a*. Oxide thickness of each sample was recorded using ellipsometer followed by the surface profiler verification. In order to fabricate the metal-oxide-silicon Carbide (MOSiC) structures, grown oxide layer on the C-face (n^+ side) was fully removed using buffer oxide etchant (BOE) by protecting the Si-face with positive photoresist. Ohmic contact was performed on the highly doped C-face with the deposition of composite layer of Ti (300 Å) and Au (2000 Å) using e-beam evaporation method in the vacuum range of 10^{-7} Torr. The grown oxide layer on Si-face of sample was retained for further processing. A cooper metal mask carrying the array of 1.0 mm diameter was employed for the selective deposition of Ni (2000 Å) on thermal oxide towards Si-face using e-beam evaporation unit in ultra high vacuum. Fig. 1, *b* shows the schematic diagram of fabricated MOSiC structures. In order to avoid environmental effect and to minimize the contact resistance, individual chip of MOSiC structures was diced using a special dicing blade from M/s DISCO Japan and packaged on TO-8 header using West Bond's ball to wedge bonder. HP 4140B pA meter/DC voltage source was used for $I-V$ measurement while 4284A LCR meter m/s Agilent technology was used for $C-V$ measurement on LabVIEW based in-house developed computer aided measurement set up. The forward current-voltage characteristics were measured by sweeping the DC bias from 0 to 5 V with 0.1 V step voltage while the reverse $I-V$ characteristics were measured by sweeping the DC bias from 0 to −100 V with 1 V step voltage. The measurement frequency and signal level for $C-V$ characteristics were fixed at 1 MHz and 1.0 V in case of high frequency, while 1 kHz and 1.0 V in case of low frequency respectively. The whole $C-V$ measurements were performed by sweeping the DC bias from −15 V to 15 V with 0.2 V step voltage.

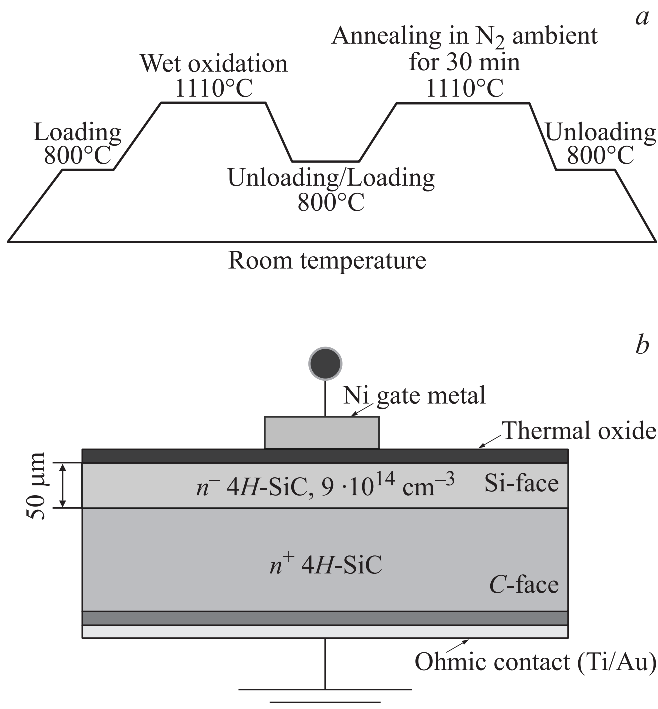

Figure 1. *a* — process flow for thermal oxidation and post oxidation annealing of 4H-SiC surface and *b* — the schematic representation of fabricated metal–oxide–Silicon Carbide (MOSiC) structure.

3. Experimental results and discussion

3.1. Effect of post oxidation annealing (POA) on current–voltage characteristics

In this section, effect of POA on forward and reverse leakage current–voltage ($I-V$) characteristics of MOSiC structure with varying oxide thickness are discussed. Fig. 2 shows the reverse current–voltage characteristics of fabricated MOSiC structure for different oxide thickness. The leakage current of both sample were analyzed across high electric field. In these calculation 4 oxide thicknesses (23.0, 36.9, 43.9 and 47.1 nm) has been taken into consideration. A strong dependency has been observed due to post oxidation annealing of oxide films, which are illustrated in Table 1. At high temperatures, N_2 having small radii penetrate to more distance in the bulk of SiO_2 and reduce the oxide defects as well as dangling bond between Si−O at the interface of SiO_2/4H-SiC. Due to this POA treatment the defect densities at the interface of SiO_2/4H-SiC as well as from bulk of SiO_2 and minority carriers were reduced, which resulted into improvement in reverse leakage current

Table 1. Reverse and forward leakage current density of MOSiC structure with varying oxide thickness at -100 and $+5$ V respectively

Oxide thickness (nm)	Reverse leakage current density at -100 V (A/cm^2)		Forward leakage current density at 5 V (A/cm^2)	
	As processed sample	Annealed sample	As processed sample	Annealed sample
17.0	–	–	$7.20 \cdot 10^{-1}$	$7.04 \cdot 10^{-1}$
23.0	$2.79 \cdot 10^{-2}$	$2.71 \cdot 10^{-7}$	$1.03 \cdot 10^{-1}$	$2.23 \cdot 10^{-8}$
36.9	$1.40 \cdot 10^{-2}$	$5.26 \cdot 10^{-7}$	$1.80 \cdot 10^{-2}$	$5.5 \cdot 10^{-9}$
43.9	$3.82 \cdot 10^{-6}$	$3.89 \cdot 10^{-7}$	–	–
47.1	$2.55 \cdot 10^{-7}$	$1.40 \cdot 10^{-7}$	$8.40 \cdot 10^{-3}$	$7.81 \cdot 10^{-4}$
56.6	–	–	$8.38 \cdot 10^{-3}$	$7.61 \cdot 10^{-4}$

of MOSiC structure as shown in Fig. 2. The observed trend in the variations of reverse leakage current is similar of all oxide thickness and its quantitative value is decreasing continuously due to the augmentation in bulk resistance of SiO_2 with the increment of oxide thickness. It has been analyzed that the reverse leakage current density at –100 V was reduced from 27.9 mA/cm^2 to 271 nA/cm^2 for oxide thickness 23.0 nm, 14 mA/cm^2 to 526 nA/cm^2 for oxide thickness 36.9 nm, 3.82 $\mu A/cm^2$ to 389 nA/cm^2 for oxide thickness 43.9 nm and 255 nA/cm^2 to 140 nA/cm^2 for oxide thickness 47.1 nm respectively due to the POA treatment.

Fig. 3 shows the forward $I-V$ characteristics of fabricated MOSiC structures for varying oxide thickness from 17.0 to 56.6 nm. This experimental plot was represented by two parts; left hand side shows the variations in forward characteristics for "As processed samples" while right hand side stands for "Annealed samples". The forward leakage current of these structures shows a strong influence of POA treatment, yielding a forward leakage current density decreases from 720 to 8.38 mA/cm^2 at $+5$ V for as processed sample while 704 mA/cm^2 to 761 $\mu A/cm^2$ same bias voltage in case of POA samples. The existence

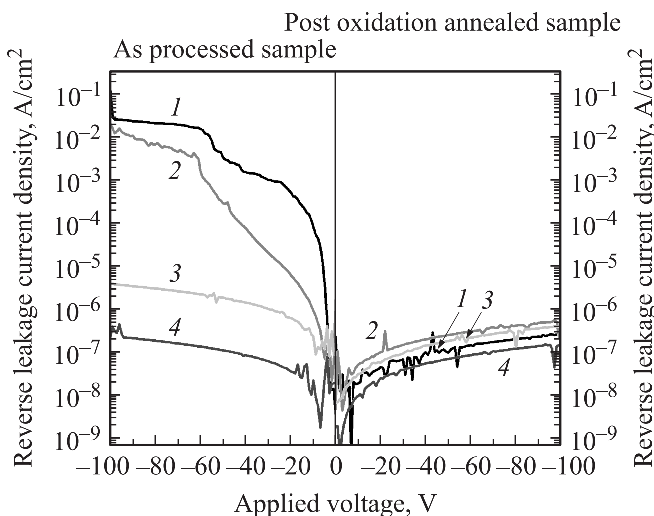

Figure 2. Reverse current–voltage ($I-V$) curves in fabricated MOSiC structure for different oxide thicknes d, nm: *1* — 23.0, *2* — 36.9, *3* — 43.9, *4* — 47.1.

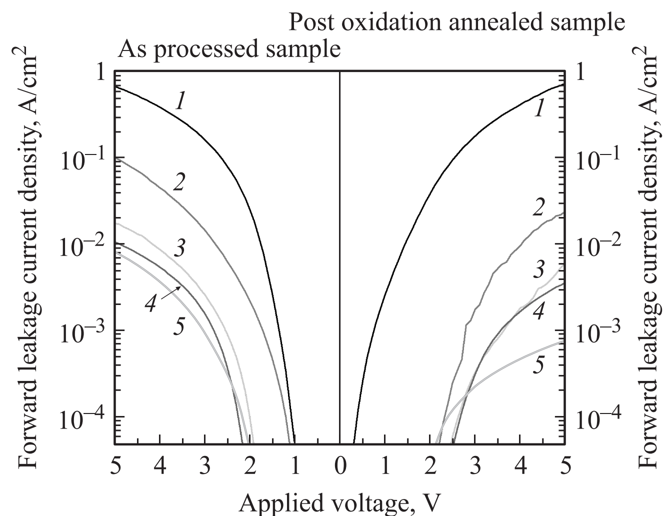

Figure 3. Forward current–voltage ($I-V$) curves in fabricated MOSiC structure for different oxide thickness d, nm: *1* — 17.0, *2* — 23.0, *3* — 36.9, *4* — 47.1, *5* — 56.6.

of meticulous gate oxide can be determined by the total amount of charge carriers that flow through the gate oxide under the influence of applied external electric field across it. There are mainly four current conduction models (Direct tunneling, Fowler–Nordheim tunneling, Schottky-emission and Poole–Frenkel conduction) available in literature [23] to describe the accurate conduction behavior based on the electrode limited or bulk limited phenomenon in metal–oxide–semiconductor (MOS) type of structures. Based on our previous experimental results [24] it has been observed that for oxide thickness range (17 to 56.6 nm) in MOSiC structure, current conduction mechanism is governed by Fowler–Nordheim (F–N) tunneling. In this reported work F–N tunneling plots were used as a tool to extract barrier height at $SiO_2/4H$-SiC interface and the POA induced leakage current was systematic studied and presented here.

The experimental data for both types of samples were fitted by Fowler–Nordheim tunneling equation which is expressed as

$$J = AE_{\text{diel}}^2 \exp\left(-\frac{B}{E_{\text{diel}}}\right), \quad (1)$$

where J is current density, E is the electric field across oxide, the pre-exponent A and slope B are given by

$$A[\mathrm{A/V^2}] = \frac{q^3 m_{\mathrm{eff}}}{8\pi m_{\mathrm{diel}} hq\Phi_B} = 1.54 \cdot 10^{-6}\, \frac{m_{\mathrm{eff}}}{m_{\mathrm{diel}}} \frac{1}{\Phi_B}, \quad (2)$$

$$B[\mathrm{V/cm}] = \frac{4\sqrt{2m_{\mathrm{diel}}(q\Phi_B)^3}}{3\hbar q} = 6.83 \cdot 10^7 \left(\frac{m_{\mathrm{diel}}}{m_{\mathrm{eff}}}\right)^{1/2} \Phi_B^{3/2}, \quad (3)$$

where q is the electronic charge, m_{eff} is the free electron mass in SiC, m_{diel} is the electron mass in the oxide, $\hbar$ is reduced Planck's constant and Φ_B is barrier height at SiO_2/SiC interface.

Fig. 4, *a* and *b* shows a linear plot of $\ln(J/E2)$ versus $1/E$ (F$-$N plot) at room temperature employing forward $I-V$ characteristics of Fig. 3. The respective value of measured slope for all oxide thickness in both set of samples shows almost same value. Using this slope, and electron effective mass in the thermal oxide of $0.55m_{\mathrm{eff}}$ [25], the effective barrier height from 4H-SiC conduction band to the oxide conduction band has been calculated as given in equation (3). Adding the 4H-SiC band gap (3.26 eV) to the calculated barrier height for all samples, confirms the band offset determined by Afanas'ev et al. [26] which is about 6 eV from the oxide conduction band to the top of the valence band in 4H-SiC. It have been further observed that the effective barrier height at SiO_2/4H-SiC interface were unaffected by oxide thickness in MOSiC structure where as a slight increment in Φ_B was examined due to POA. The variations in the values of effective barrier height were illustrated in the inset of Fig. 5. The reduction in forward leakage current due to POA may well explain on the basis of this observed effective barrier height. It is believed that the densities of carbon-oxides, which are being trapped at the interface of SiO_2/4H-SiC during thermal oxidation process, were reduced due to high temperature POA. As the result, the barrier height at the interface (SiO_2/4H-SiC) will be increased due to rearrangement of pure SiO_2 at the interface. As the effective barrier height increases, the current density, at a given electric field decreases significantly with positive polarity of gate bias. This is because of the conduction electrons which suffer more energy barrier. Since all POA samples have higher effective barrier height compared to as processed samples, the forward leakage current was significantly reduced.

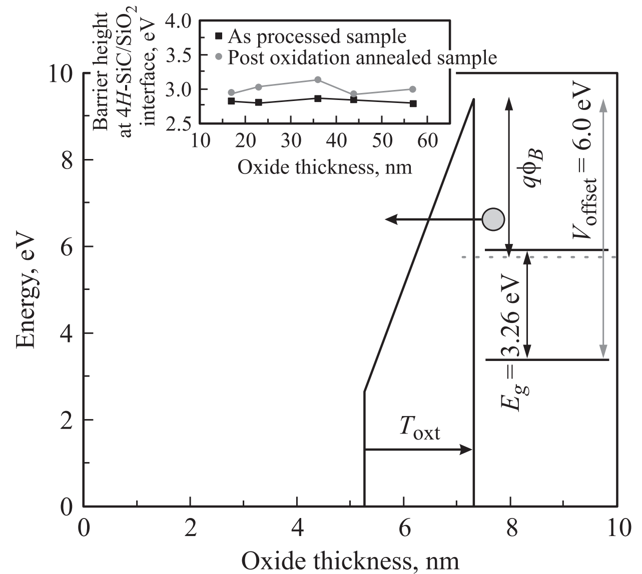

Figure 5. Energy band diagram of MOSiC structure with oxide thickness variations in strong accumulation condition (high $+V_e$ voltage at gate) and inset show the variations of effective barrier height at SiO_2/4H-SiC interface as a function of oxide thickness for as processed as well as post oxidation annealed samples.

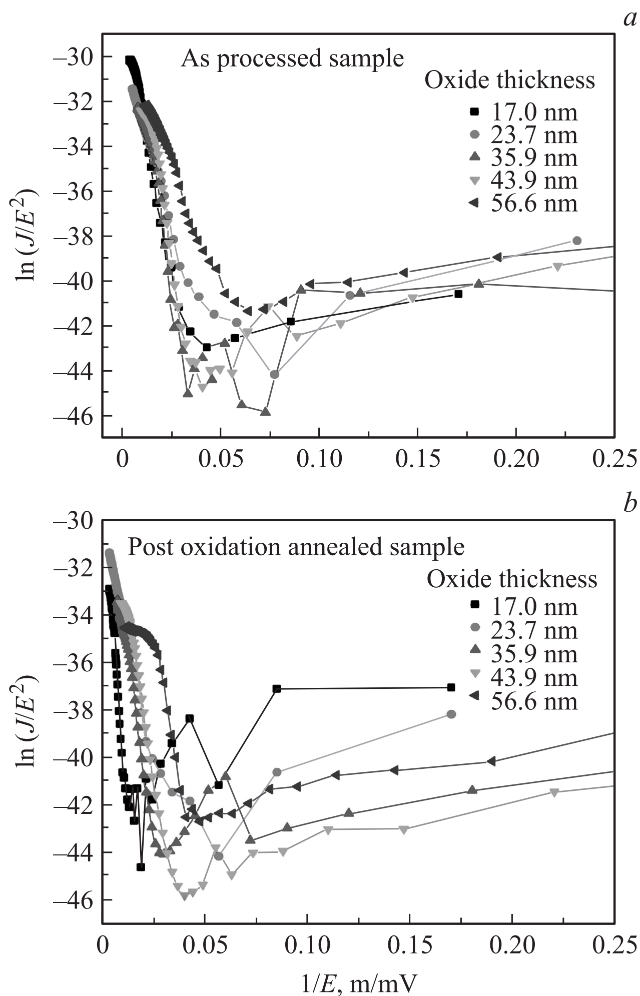

Figure 4. *a* — Fowler–Nordheim plots for *n*-type 4H-SiC based MOSiC structure obtained from forward $I-V$ measurement of as processed sample and *b* — for post oxidation annealed samples.

3.2. Effect of post oxidation annealing (POA) on capacitance–voltage ($C-V$) characteristics

In this section, effect of POA on $C-V$ characteristics of MOSiC structure with varying oxide thickness was discussed. The two type of oxide charges (fixed oxide

charge and oxide trapped charge) were calculated from experimental $C-V$ curves for both cases. Fig. 6 shows the typical high frequency $C-V$ curve of POA samples with varying oxide thickness in MOSiC structure. The variation of oxide thickness was taken from 17 to 66.1 nm. The flat band voltage was calculated by comparing the ideal $C-V$ curve to the experimentally measured curve for all oxide thickness. The variation in the flat band voltage shifts was presented in Fig. 7. The increment in the positive flat band voltage shift with oxide thickness was considered to be caused by the increment of negatively charged electron during the process.

In the extraction of fixed charges (Q_{fix}) as well as oxide trapped charges (Q_{oxt}), it has been observed that oxide thickness plays a significant role. In both the cases, a deep acceptor-type interface state appears which were mainly

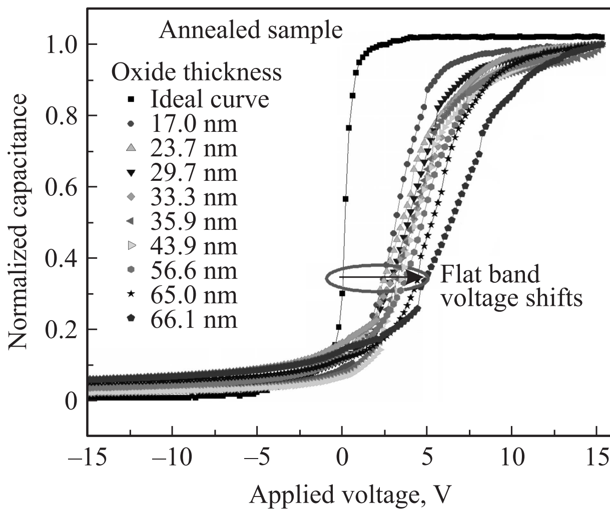

Figure 6. Flat band voltage shifts from an ideal curve of annealed oxide in N_2 ambient for different oxide thickness in MOSiC structure.

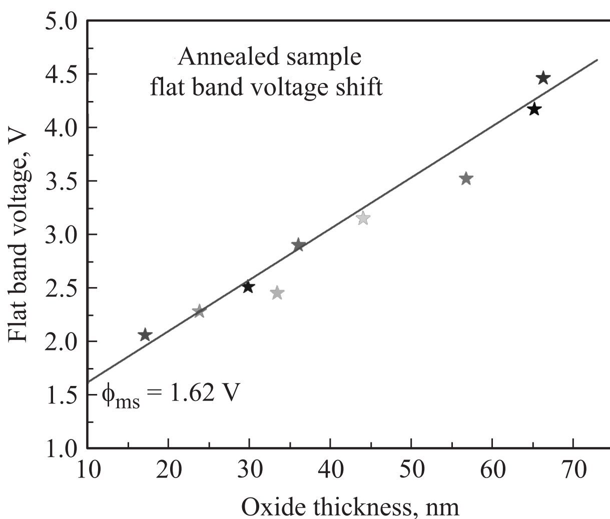

Figure 7. Variation of flat band voltage with oxide thickness for post oxidation annealed oxide in MOSiC structure.

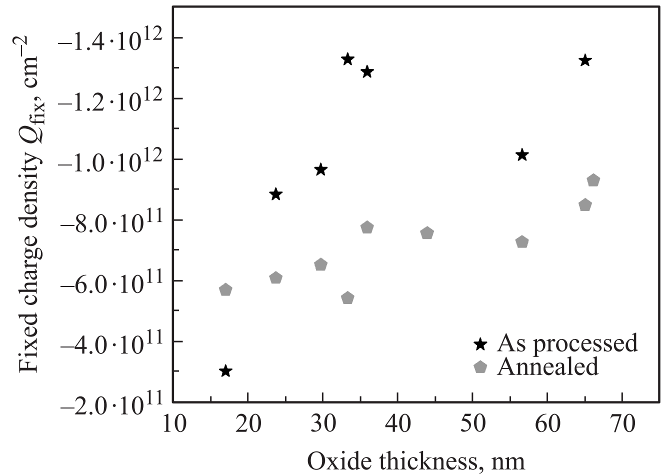

Figure 8. Distributions of fixed charge densities as a function of oxide thickness for both samples i. e. as processed oxides and post oxidation annealed oxide.

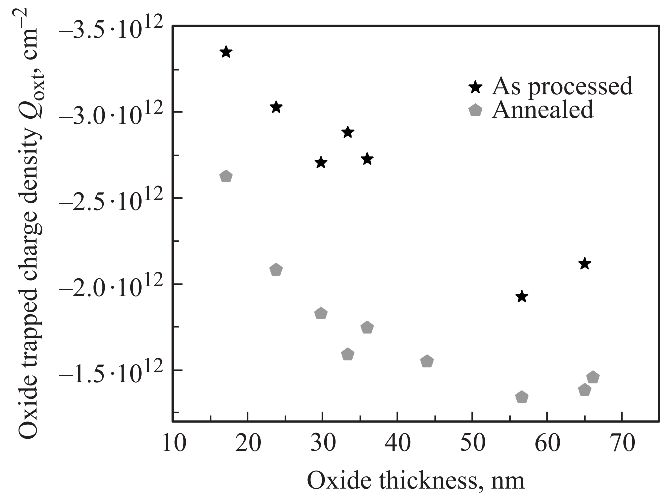

Figure 9. Distributions of oxide trapped charge densities as a function of oxide thickness for both sample i. e. annealed and as processed oxides.

caused by real oxide charges and electrons, captured at the interface of $SiO_2/4H$-SiC. The all experiments were repeated several times to confirm the results obtained in Fig. 8 and 9. Flat band voltage, fixed oxide charge density and oxide trapped charge density extracted from high frequency $C-V$ curve for "As processed" and "Annealed sample" are listed in Table 2. Using the measured flat band voltage shift for known oxide capacitance, negative fixed charge densities were estimated, which varies from $-3.42 \cdot 10^{11}$ to $-1.02 \cdot 10^{12}\,\text{cm}^{-2}$ for as processed sample while from $-5.66 \cdot 10^{11}$ to $-9.31 \cdot 10^{11}\,\text{cm}^{-2}$ in case of vacuum annealed samples. In both cases these variations shows a parabolic trend. During the initial growth of SiO_2, carbon-oxides were trapped at $SiO_2/4H$-SiC interface [27] and caused a fixed oxide charge. When oxide thickness increases (for higher oxidation time), the trapped carbon-

Table 2. Flatband voltage, fixed oxide charge density and oxide trapped charge density extracted from high frequency $C-V$ curve for „As processed“ and „Annealed sample“

Oxide thickness (nm)	Flat band voltage (V)		Fixed oxide charge density (cm^{-2})		Oxide trapped charge density (cm^{-2})	
	As processed sample [24]	Annealed sample	As processed sample	Annealed sample	As processed	Annealed sample
17.0	2.64	2.07	$-3.04 \cdot 10^{11}$	$-5.71 \cdot 10^{11}$	$-3.34 \cdot 10^{12}$	$-2.62 \cdot 10^{12}$
23.7	3.40	2.29	$-8.85 \cdot 10^{11}$	$-6.09 \cdot 10^{11}$	$-3.02 \cdot 10^{12}$	$-2.08 \cdot 10^{12}$
29.7	–	2.52	$-9.66 \cdot 10^{11}$	$-6.53 \cdot 10^{11}$	$-2.70 \cdot 10^{12}$	$-1.83 \cdot 10^{12}$
33.3	–	2.46	$-1.32 \cdot 10^{12}$	$-5.44 \cdot 10^{11}$	$-2.88 \cdot 10^{12}$	$-1.59 \cdot 10^{12}$
35.9	4.45	2.91	$-1.29 \cdot 10^{12}$	$-7.75 \cdot 10^{11}$	$-2.72 \cdot 10^{12}$	$-1.74 \cdot 10^{12}$
43.9	4.54	3.16	–	$-7.56 \cdot 10^{11}$	–	$-1.55 \cdot 10^{12}$
56.6	5.06	3.53	$-1.01 \cdot 10^{12}$	$-7.27 \cdot 10^{11}$	$-1.92 \cdot 10^{12}$	$-1.34 \cdot 10^{12}$
65.0	–	4.18	$-1.32 \cdot 10^{12}$	$-8.49 \cdot 10^{11}$	$-2.12 \cdot 10^{12}$	$-1.38 \cdot 10^{12}$
66.1	–	4.47	–	$-9.30 \cdot 10^{11}$	–	$-1.45 \cdot 10^{12}$

oxides in the bulk of grown SiO_2 is significantly increased. However, this increment has a limitation. As oxide thickness increases further, the bulk resistance of oxide will not allow further diffusion of oxidizing agent towards the 4H-SiC surface. As a result of this the formation of carbon-oxide will become constant and the nature of the curve was seemed to be parabolic (Fig. 8). However, on other hand Q_{oxt} decreases linearly having negative magnitude as oxide thickness increases. It is believed that the maximum effective trapped charge density in n-type MOSiC structures are limited by acceptor traps, falling below the Fermi level. These results can be also explained in terms of generation of acceptor traps in the upper half of the band gap. Basically, Q_{oxt} are originated by the trapping of electrons and holes during thermal oxidation process [28]. Some of these positively charged holes are recombined with negative fixed oxide charged and become neutral at the interface. As oxide thickness increases further these recombination process become more effective because fixed charges have incremental trend with oxide thickness. As the result, the effective oxide trapped charges will be reduced. These reductions in the oxide trapped charge as a function of oxide thickness were illustrated in Fig. 9.

In the process of POA, molecular nitrogen was taken as annealing ambient due to two reasons; creation of $Si\equiv N$ bonds at the $SiO_2/4H$-SiC interface that passivate (a) interface traps due to dangling and strained bonds and (b) it act as a barrier for removal of carbon-oxides and other complex silicon oxides compounds. Since, 4H-SiC and SiO_2 interface have higher mismatch, so the incorporation of molecular nitrogen during POA can reduce stress between SiC and oxide. The influence of surface passivation and reduction of stress in thermal oxide film was confirmed by the variation of Q_{fix} and Q_{oxt} with oxide thickness. The POA treated samples were compared with as processed sample. Continuous reductions in fixed charge density as well as oxide trapped charge density were investigated (Fig. 8 and 9). Symbol „star“ shows the variation of as processed samples while the symbol „pentagon“ shows the variation of POA samples.

4. Conclusions

In this paper, a systematic study of the effect of post oxidation annealing (POA) on $I-V$ and $C-V$ characteristics of metal–oxide–silicon carbide (MOSiC) systems on 4H-SiC (0001) substrate has been systematically investigated and reported. POA had a noticeable effect on oxide charges and reverse leakage current. It has been analyzed that the reduction in the defect densities at the interface of $SiO_2/4H$-SiC and lower minority carriers due to POA resulted into improved reverse leakage current. Reduction in the forward leakage current was analyzed on the basis of increment in the effective barrier height at $SiO_2/4H$-SiC interface. Surface passivation and reduction in stress of thermal oxide film was also verified in the variation of Q_{fix} and Q_{oxt} with oxide thickness. The developed process has direct impact in the fabrication of SiC based MOS devices/structures.

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