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Study of the temperature dependence of the light-voltage-current characteristics of silicon heterojunction solar cells

© E.I. Terukov[1–4], O.K. Ataboev[5], D.A. Malevskiy[1], I.E. Panaiotti[1], A.V. Kochergin[3], I.S. Shakhray[4]

[1] Ioffe Institute, St. Petersburg, Russia
[2] ITMO University, St. Petersburg, Russia
[3] R&D Center of Thin Film Technologies in Energetics under the Ioffe Institute LLC, St. Petersburg, Russia
[4] St. Petersburg State Electrotechnical University „LETI", St. Petersburg, Russia
[5] Research Institute of Semiconductor Physics and Microelectronics, National University of Uzbekistan named after Mirzo Ulugbek, Tashkent, Uzbekistan
E-mail: e.terukov@hevelsolar.com

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A study of the temperature dependence of the light volt-ampere characteristics of silicon heterojunction solar cells made on *n*- and *p*-type silicon substrates in a wide temperature range (from -100 to $+100\,^\circ$C) has been carried out. The observed difference in the behavior of the light volt-ampere characteristics is explained by the peculiarities of the energy band diagrams of the silicon heterojunction solar cells.

Keywords: silicon solar cell, heterojunction solar cells, temperature dependence of the current-voltage characteristics, *S*-shaped current-voltage characteristics.

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In recent decades, solar energy has become a promising and environmentally friendly component of the electrical power generation industry. Among silicon-based solar cell (SC) technologies, heterojunction solar cells (HJT SCs) have attracted the most attention, since they offer excellent surface passivation, high open-circuit voltages, and record-high efficiencies, which reach 27.3 % in industrial SC production [1]. In practice, *n*-type silicon substrates, which provide a higher efficiency than *p*-type ones, are used to manufacture terrestrial HJT SCs. However, the use of silicon cells in solar batteries for spacecraft requires a transition to *p*-type silicon substrates, since they are less sensitive to irradiation. The operating temperature of solar batteries in orbit varies from -100 to $+100\,^\circ$C, and one needs to determine the behavior of solar cells within this temperature range in order to predict the performance parameters of such batteries.

Current-voltage characteristics (CVCs) are one of the main diagnostic tools for evaluating photovoltaic parameters and clarifying the mechanisms of current flow in SCs [2]. Ideal light CVCs are normally rectangular and are shaped by the values of short-circuit current density (J_{sc}), open-circuit voltage (V_{oc}), and fill factor (FF), which determine together the level of efficiency (η). Under real operating conditions, non-ideal behavior is often observed, which is manifested in CVC distortions. These distortions serve as critical indicators of efficiency reduction mechanisms [3]. It is known [3–5] that an *S*-shaped CVC is observed for HJT SCs on *n*-type silicon substrates. This effect is attributed to the features of the energy band diagram of an HJT SC on an *n*-type silicon substrate [6,7] or to the design features of a solar cell, such as transparent conductive layers on the HJT SC surface [8]. In addition, it was found that *S*-shaping become less pronounced with increasing temperature [9], which is also indicative of influence of the barrier effect in charge transfer. Data on the behavior of light CVCs in HJT SCs on *p*-type substrates within a wide temperature range have not been presented to date.

The present study is focused on the examination of influence of temperature on this effect in HJT SCs on *n*- and *p*-type substrates.

HJT SC samples (Fig. 1) were fabricated on Czochralski-grown *n*- or *p*-type crystalline silicon substrates with a thickness of $\sim 125\,\mu$m doped with phosphorus and gallium. The carrier density in the substrate was $\leqslant 10^{16}\,\mathrm{cm}^{-3}$.

Films of *p*- and *n*-type amorphous hydrogenated silicon *a*-Si:H with a thickness of 10–15 nm, which were grown on top of a thin (~ 7 nm) buffer $(i)a$-Si:H layer with intrinsic conductivity, formed heterojunctions on the surfaces of *n*- or *p*-type crystalline silicon wafers. The formation of buffer layers of amorphous hydrogenated silicon with intrinsic conductivity in the structures of modern HJT SCs is aimed at reducing the rate of surface recombination. This technological approach allows for effective passivation of the silicon wafer surface after chemical treatment, and the resulting recombination losses in HJT SCs are then determined almost entirely by the lifetime of carriers in the substrate [10].

Samples with an area of $1\,\mathrm{cm}^2$ cut from HJT SCs produced by OOO „NTTs TPT" were examined without subsequent passivation of lateral surfaces.

A collimated light flux produced by a pulsed simulator with the AM0 spectrum and an energy density of

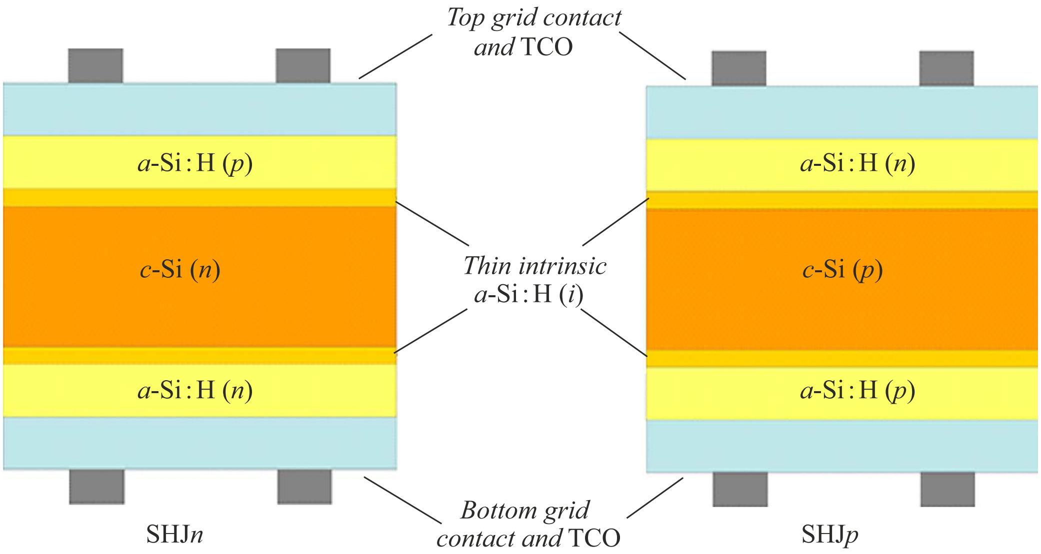

Figure 1. Structure of HJT SC samples with n- or p-type bases.

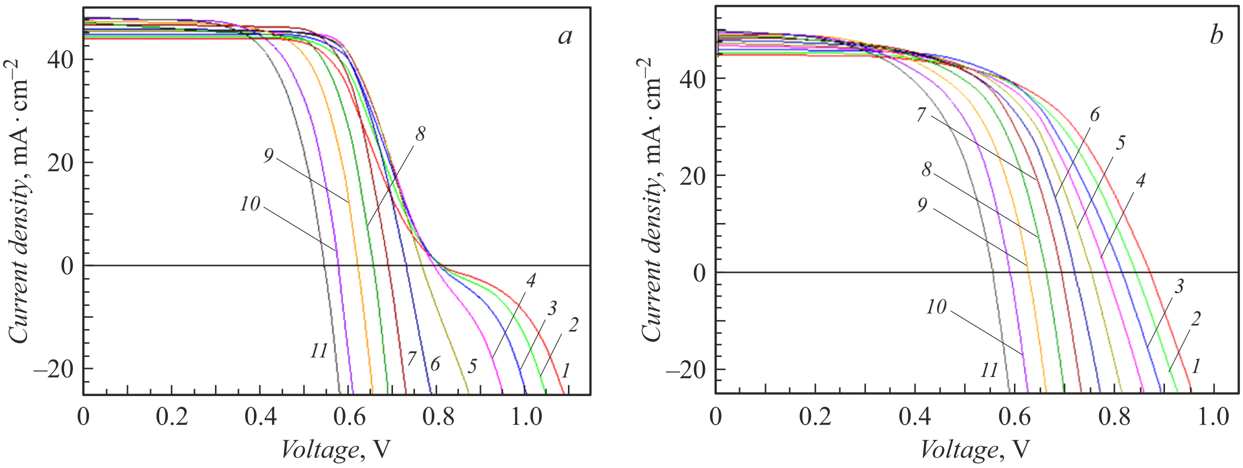

Figure 2. Light CVCs of HJT SCs based on n-type (a) and p-type (b) c-Si substrates in the AM0 spectrum (1367 W/m^2) within the range of temperatures T from -100 to $+100\,^\circ$C. $T = -100$ (*1*), -80 (*2*), -60 (*3*), -40 (*4*), -20 (*5*), 0 (*6*), +20 (*7*), +40 (*8*), +60 (*9*), +80 (*10*), +100 °C (*11*).

1367 W/m^2 was used to measure the temperature dependences of light CVCs in a nitrogen cryostat.

The experimental light CVCs of HJT SCs on p- and n-type crystalline silicon substrates are shown in Fig. 2.

It can be seen from the figure that the light CVCs of the sample fabricated on an n-type substrate become S-shaped at temperatures below $-40\,^\circ$C, which leads to a significant reduction in fill factor FF and photovoltaic conversion efficiency η. However, this effect is not observed if the HJT SC is fabricated on a p-type substrate. Similar experimental results for an n-type substrate have already been reported earlier (see, e.g., [3,11]).

In our view, the S-shaped appearance of light CVCs of HJT SCs on n-type substrates at low temperatures is attributable to the specific features of the energy band diagrams of their semiconductor structures (Fig. 3). The discontinuities of conduction (ΔE_C) and valence (ΔE_V) bands were estimated based on the well-known Anderson model [12]. Calculations were performed with the use of electron affinity values of 4.05 eV for c-Si and 3.09 eV for a-Si:H [13].

$$\Delta E_V = (E_{g1} - E_{g2}) - \Delta E_C, \tag{1}$$

where $E_{g1} = 1.72$ eV and $E_{g2} = 1.12$ eV are the band gaps of a-Si:H and c-Si, respectively, at room temperature [13]. The data from [14] were used to estimate the band gap of thin layers of amorphous silicon a-Si:H.

When the temperature decreases, the values of E_{g1} and E_{g2} change so that their difference $E_{g1} - E_{g2}$ and, consequently, valence band discontinuity $\Delta E_V(T)$ (1) increase [15,16]. In the case of an n-type substrate, $\Delta E_V = 0.45$ eV at room temperature. As T decreases, the height of potential barrier $\Delta E_V(T) > 0.45$ eV for minority carriers at the boundary of the a-Si:H/(n)c-Si heterojunction

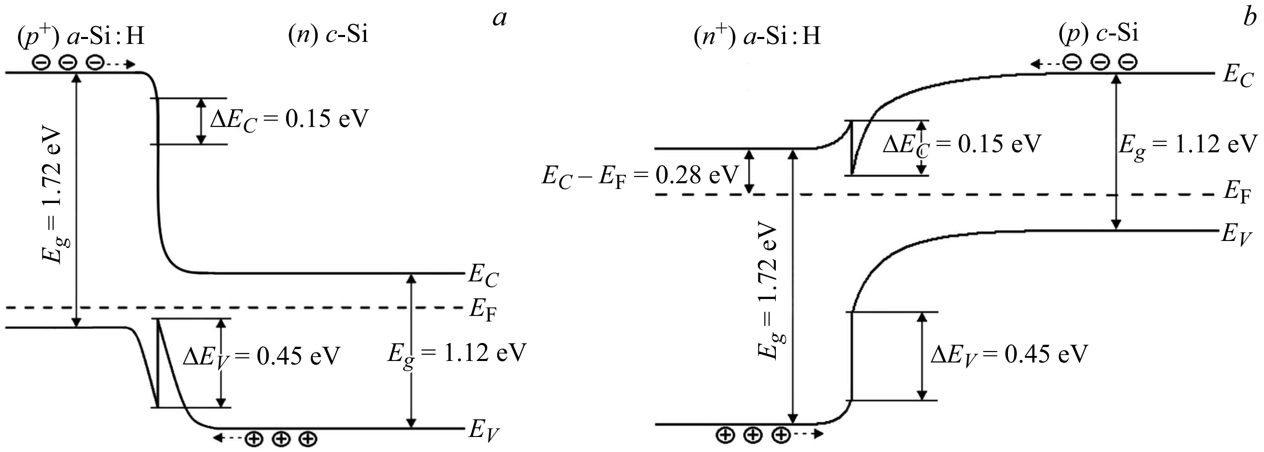

Figure 3. Room-temperature energy band diagrams of the semiconductor structures of HJT SCs based on n-type (a) and p-type (b) crystalline substrates. Electrons and holes are denoted by symbols ⊖ and ⊕, respectively.

increases. At $T < 40\,^\circ$C, the fraction of holes penetrating from c-Si to a-Si:H decreases significantly due to active accumulation of holes in the potential well at the left surface of an n-type substrate. This impediment of transport of minority carriers through the potential barrier is what causes the emergence of S-shaped CVCs of HJT SCs with n-type crystalline silicon substrates.

In the case of a p-type substrate, minority carriers (electrons) overcome a relatively low potential barrier, which is just 0.15 eV in height at room temperature, at the Si:H/$(p)c$-Si heterojunction boundary. Even at low temperatures, this barrier does not impede the transport of carriers from the substrate to the amorphous silicon layer in any significant way, since the accumulation of electrons is barely noticeable. Therefore, the CVCs of HJT SCs with p-type crystalline silicon substrates are not S-shaped.

Thus, it was demonstrated that S-shaped light CVCs of HJT SCs arise due to the specific features of the energy band diagrams of semiconductor structures fabricated on silicon substrates of different conductivity types.

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Conflict of interest

The authors declare that they have no conflict of interest.

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