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Synchronization system for quantum key distribution devices

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In commercial quantum key distribution (QKD) systems, high synchronization accuracy between the reference oscillators of the transmitter and receiver plays a key role in ensuring proper operation. An implementation of a frequency difference correction system for a QKD device is proposed. The paper describes in detail an optical synchronization scheme, two-stage frequency correction method and noise-resistant method for automatic determination of the quantum state reception and transmission start time on the receiver and transmitter. To validate the proposed technical solutions, a series of experiments was carried out using a real QKD device implementing the BB84 protocol. As a result, stable operation of all components of the proposed frequency difference correction system was demonstrated. Stabilization accuracy provides reliable distribution of secret keys between remote nodes.

Keywords: reference oscillator stability, frequency synthesizer, time and wavelength division multiplexing, metastability, phase error, M sequence, synchronization, quantum key distribution.

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Introduction

Quantum key distribution (QKD) is a promising technique providing safe cryptographic key exchange [1,2]. In most proposed QKD protocols, two remote parties — transmitter (Alice) and receiver (Bob) — generate a shared secret key by sharing quantum states via an optical channel. Key security is ensured by the quantum mechanics principles. In particular, due to a probabalistic nature of quantum measurements, an attempt to intercept transmitted quantum states by a third party (Eve) will introduce noise in them, which will be detected by Alice and Bob [3,4]. The received secret key can be later used in classical encryption schemes [5].

Modern QKD devices demonstrate secret key generation rate and range sufficient for practical application [6–8]. However, technical difficulties associated with their implementation significantly restrict potential large-scale deployment of these devices in existing communication networks. One of such difficulties includes the problem of stable synchronization of operating frequencies of nodes participating in the key distribution process [9–11]. Operating frequency synchronization is necessary because the receiver and transmitter, for preparing and recording quantum states, generally use independent reference oscillators (RO) required for generating the frequency synthesizer reference frequency. Synthesizers use the reference frequency to generate a set of output signals, which represent operating frequencies of the device. Difference of reference frequencies will apparently result in failure to generate secret keys [12]. The current level of reference oscillator manufacturing process makes it impossible to produce generators with identical output frequencies. In addition, generators are prone to temperature and physical impacts, and gradual ageing. As a result, even the best of available reference oscillators don't have sufficient stability for use without periodic frequency difference compensation [13–15].

Owing to the lack of uniform approach, most existing high frequency QKD devices on the market implement their own unique synchronization systems satisfying the requirements of a particular device. They most often use optical signals to transfer information about the current frequency of the master node with Alice's reference oscillator usually chosen as the master node [16–18]. Then, Bob uses the received information to calculate the frequency difference and adjust his reference oscillator. Additional optical fiber, atmospheric channel or the same optical fiber as for quantum state transmission (quantum channel) may be used as an optical channel for clock signal transmission. In the latter case, time division multiplexing (TDM) or wavelength division multiplexing (WDM) methods can be used to isolate quantum states from high-power synchronization radiation [19–21].

A widely used approach includes using a sequence of high-power optical pulses as a synchronization signal (synchronization sequence) [17,22,23]. By analyzing this sequence, Bob can get information about transmitter frequency and use it to determine the frequency difference. For correct registering of quantum states, it is necessary not only

to compensate the operating frequency difference between the receiver and transmitter, but also to synchronize their phases. Consequently, either a quantum state preparation frequency or frequencies obtained by multiplying or dividing this frequency by integer coefficients may be used as a pulse repetition frequency in the synchronization sequence because such frequencies retain rigid phase coupling with the initial frequency.

Another approach uses correlation between the sent and received signal quantum state sequences to calculate the current frequency difference between Alice's and Bob's generators [11,24,25]. For example, in [25], the transmitter regularly sent a qubit synchronization sequence, which was known by the receiver in advance. Then, by calculating the autocorrelation function (ACF) between its copy and the received synchronization sequence, the receiver determined a time delay between the sent and received quantum states. In addition, this sequence is not used for secret key generation and, thus, device security is not affected. Apart from special qubit sequences, such systems may use public information disclosed by Alice and Bob at the raw key sifting stage, for example, qubit bases and types [11].

This paper proposes a synchronization system for QKD devices implementing discrete-variable protocols. This synchronization system can be represented as a hardware and software complex consisting of three main components:

1) optical synchronization scheme;

2) set of methods for correction of operating frequency difference between the receiver and transmitter;

3) method for alignment of optical pulse reception and transmission start times on each of the nodes.

Implementations of components 2 and 3 proposed in this work haven't been discussed in detail in the literature in terms of utilization in synchronization systems for QKD devices. This work describes the developed synchronization system using the case of implementation for a commercial BB84-based QKD device [16]. Section 1 provides a brief review of the given QKD device to define the synchronization system requirements. Section 1 also describes the employed optical synchronization scheme. Section 2 describes the analysis of the parameters of the frequency oscillators used in the device and comparative analysis of operating frequency tuning methods. Further, a two-stage algorithm of operating frequency difference compensation based on synchronization of the receiver and transmitter reference frequencies is described. Section 2.1 describes in detail a method of quick frequency difference compensation in QKD devices using digital asynchronous variable-length buffers. Section 2.2 addresses in detail the proposed method of using digital trigger metastability and signal jitter phenomenon for keeping the constant phase difference between Alice's and Bob's operating frequencies. In Section 3, a method based on calculating the M sequence autocorrelation function was proposed and tested to enable noise-resistant alignment of optical pulse reception and transmission start times on the receiver and transmitter. Comprehensive study of the implemented synchronization system parameters, including accuracy and stability, was conducted on various quantum channel lengths as part of the BB84-based QKD device. All test results are provided in Section 4.

1. Optical synchronization scheme

As mentioned above, a particular synchronization system implementation is chosen in accordance with the parameters of the QKD device, for which the system is being designed. In this case, it is necessary to consider the implemented QKD protocol, hardware and software components used in the device, and device's optical scheme. Figure 1, *a* shows the optical scheme of the given QKD device implementing the BB84 protocol with polarization encryption [22].

Device hardware components are operated by a Xilinx Virtex-7 FPGA board. Signal optical pulse generation frequency is $f_{prep} = 312.5$ MHz. This and other frequencies used in the device are generated using the Silicon Labs Si5340 frequency synthesizer, which uses a voltage-controlled high-stable temperature-stabilized reference oscillator with nominal frequency 10 MHz as a reference source.

In the proposed synchronization system, the transmitter with T_{rep} generates a synchronization sequence to transmit information about the current frequency of its reference oscillator. A quantum channel is used as an optical channel for transmitting this sequence. However, fiber transmission of high-power clock signals is followed by an increase in the SPD receiver exposure level due to Raman and Rayleigh scatterings in optical fiber, and by reflections on welding and joint defects. A TDM method where high-power synchronization sequence and quantum state sequence are sent at different times, avoiding the effect of classical radiation on SPD is used to minimize exposure contribution. Scheme of using the TDM method for sending the synchronization sequence with the repetition period T_{rep} is shown in Figure 1, *b*. Disadvantage of this approach is in reduction of secret key generation rate due to the appearance of synchronization time windows. To isolate SPD from the synchronization sequence radiation, noise exposure and multiple reflections in fiber, our synchronization system also uses the WDM method.

Optical scheme of the device shown in Figure 1, *a*, includes the optical scheme for quantum state preparation and measurement and optical synchronization scheme [22]. The latter consists of pulse laser L2, photodetector SD, tunable optical attenuator VOA2 and filters WDM1 and WDM2. Laser L2, which is operated using an additional transceiver on the FPGA board, is used to generate a synchronization sequence on the transmitter. Receiver-side photodetector SD in turn converts the received synchronization sequence to electric signal for further processing.

To implement the WDM method, DWDM filters (WDM1 and WDM2) are installed in the receiver and transmitter. Bandpass of the filters corresponds to the signal laser

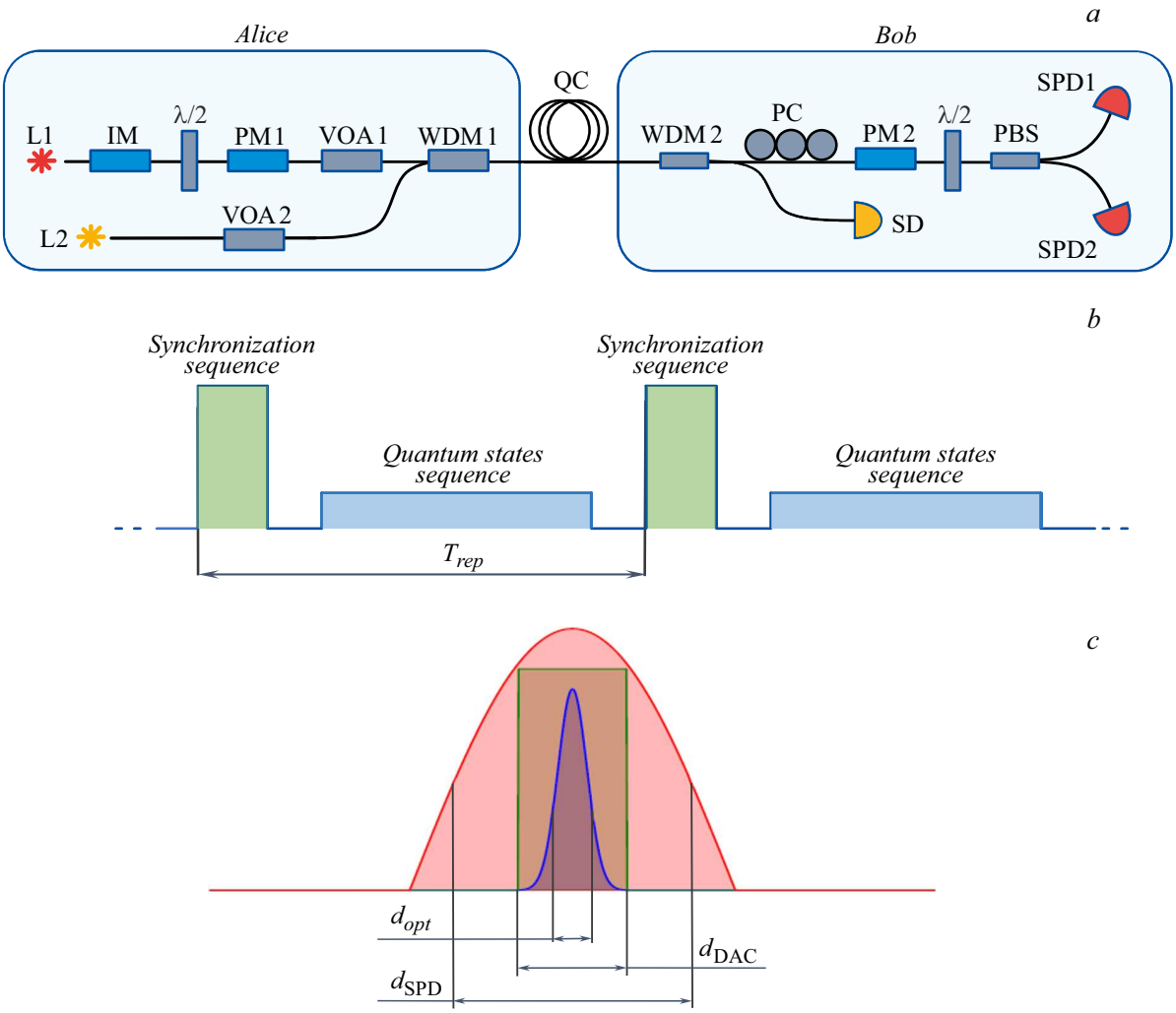

Figure 1. *a* — optical scheme of the receiver and transmitter of the QKD device with polarization encryption. L1 — signal laser, IM — intensity modulator, $\lambda/2$ — half-wave plate, PM1 and PM2 — phase modulators, VOA1 and VOA2 — variable optical attenuators, PC — polarization controller, PBS — polarizing beam splitter, SPD1 and SPD2 — single-photon gate detectors, QC — quantum channel (single-mode dark optical fiber), L2 — synchronization laser, WDM1 and WDM2 — optical filters, SD — synchronization detector. *b* — scheme of using the TDM method for sending synchronization sequence with repetition period T_{rep}. *c* — diagram of time overlapping of the phase modulator pulse, SPD gate and signal laser pulse. d_{SPD} — SPD gate width, d_{opt} — optical pulse width, d_{DAC} — modulation pulse width.

wavelength — 1548.5 nm (36 DWDM channel). Laser L2 wavelength was set to 1554.25 nm (28 DWDM channel).

When the quantum channel is changed, optical loss in it can also change, which necessitates correction of synchronization system parameters, in particular, of the synchronization laser and synchronization detector. Optimal parameter choice directly defines synchronization quality. To arrange switching between the lines with different loss, variable optical attenuator VOA2 was added to the optical scheme to maintain the constant level of loss between the synchronization laser and synchronization detector independently of the loss in the fiber optic line.

Since the synchronization sequences are sent with period T_{rep}, frequency correction procedure shall be also fulfilled at regular intervals T_{corr}, and generator phase difference between the receiver and transmitter during time T_{corr} shall not exceed the threshold value $\Delta\varphi^{\max}$, at which proper functioning of the QKD devices is disrupted. The period between the nearest corrections T_{corr} is in turn limited at the bottom by the synchronization sequence sending period ($T_{rep} \leq T_{corr}$) and is defined by the quality of reference frequency generators used in the QKD device, however, the allowable value of T_{corr} doesn't exceed some seconds even for the best available models.

Hereinafter for convenience of time parameter analysis and calculations involving these parameters, instead of $\Delta\varphi^{\max}$ we use a corresponding time shift between the receiver and transmitter reference frequency cycles $\Delta t^{\max}$, which is defined as:

$$\Delta t^{\max} = \frac{\Delta\varphi^{\max}}{2\pi f_{gen}},$$

where f_{gen} is the nominal generator frequency. To find $\Delta t^{\max}$, consider in more detail the process of optical pulse receiving by the receiver, including device time parameters. Before starting the secret key generation, primary device calibration procedure is carried out. In particular, for correct receiving of optical pulses, SPD1 and SPD2 gate delays shall be set. Also, the turn-on delay of modulator PM2 shall be aligned in accordance with the optical pulse arrival time. Lack of or partial modulation of optical pulse will result in failure to properly receive quantum states due to the increase of the quantum error (QBER). Figure 1, *c* shows the diagram of overlapping between the optical pulse and receiver control pulses, which is derived from successful delay calibration. In the given QKD device, the optical pulse width $d_{\text{opt}} \approx 150$ ps, SPD gate width $d_{\text{SPD}} \approx 800$ ps, used modulation pulse width $d_{\text{DAC}} \approx 400$ ps. As shown in Figure 1, *c*, receiver and transmitter frequency cycle difference by more than 100 ps is sufficient for the optical pulse to go beyond the modulating pulse of PM2. Consequently, the maximum allowable time shift between the receiver and transmitter reference frequency cycles during the correction period shall meet the condition $\Delta t^{\max} \leq 100$ ps. When developing our synchronization system, $\Delta t^{\max} = 100$ ps was used as the target parameter.

2. Receiver and transmitter frequency difference correction methods

As mentioned in Section 1, the proposed synchronization methods provide correction of the receiver frequency in accordance with the transmitter frequency with the predefined period T_{corr}. To determine the maximum allowable value $T_{corr}^{\max}$, consider the possible total frequency deviation of one reference oscillator from the nominal frequency Δf_{gen} defined as a set of additive components:

$$\Delta f_{gen} = \Delta f_{def} + \Delta f_{res} + \Delta f_{temp} + \Delta f_{vcc},$$

where Δf_{def} is the initial generator frequency accuracy; Δf_{res} is the power-up generator frequency deviation (stability); Δf_{temp} is the generator frequency deviation (stability) associated with temperature fluctuations; Δf_{vcc} is the generator frequency deviation (stability) resulting from control voltage fluctuations.

Typical (mean) values of the deviations listed above, in ppm (parts per million of f_{gen}), are provided in the technical documentation of reference oscillator used in the device:

- initial accuracy $P_{def} = \pm 0.1$ ppm;
- power-up frequency stability $P_{res} = \pm 10 \cdot 10^{-3}$ ppm;
- frequency stability from temperature: $P_{temp} = \pm 0.1 \cdot 10^{-3}$ ppm;
- frequency stability from control voltage: $P_{\text{vcc}} = \pm 0.2 \cdot 10^{-3}$ ppm.

Note that the given values are also valid for all derivative frequencies formed from the initial generator frequency. Note that the deviation Δf from f_{gen} (with the periodT_{gen}) and the corresponding deviation ΔT from the nominal period T_{gen} are calculated as:

$$\Delta f = \frac{f_{gen} \cdot P}{10^6} \tag{1}$$

and

$$\Delta T = \frac{T_{gen} \cdot P}{10^6}, \tag{2}$$

where one of the values listed above should be substituted instead of Δf and P. Since the initial generator frequency deviation from P_{def} and power-up frequency deviation P_{res} shall be compensated only once when the QKD device is started, generator frequency stability during operation of the device P_{work} is defined only by temperature and power voltage stability, so the working frequency deviation may be written as:

$$P_{work} = P_{temp} + P_{vcc} = \pm 0.3 \cdot 10^{-3} \text{ ppm}.$$

It follows from expressions (1) and (2) that the worst-case total absolute reference frequency (or period) difference of two reference oscillators during device operation (with f_1 and f_2, respectively) is defined as:

$$|f_2 - f_1| = |(f_{gen} + \Delta f_{work} + \Delta f_{\text{const}}) - (f_{gen} - \Delta f_{work})| = \frac{2 f_{gen} \cdot |P_{work}|}{10^6} + \Delta f_{\text{const}}, \tag{3}$$

where Δf_{work} is the typical nominal frequency deviation due to reference oscillator instability during device operation, Δf_{const} is the current intentional frequency difference. Since $\Delta f_{\text{const}} = 0$ during normal operation of the QKD device, expression (3) is reduced to:

$$|f_2 - f_1| = |(f_{gen} + \Delta f_{work}) - (f_{gen} - \Delta f_{work})| = \frac{2 f_{gen} \cdot |P_{work}|}{10^6}. \tag{4}$$

Accumulation of the difference of the numbers of generated cycles is the consequence of reference oscillator frequency deviation by Δf_{work} during time t :

$$|N_2 - N_1| = |f_2 \cdot t - f_1 \cdot t| = 2|\Delta f_{work}| \cdot t = \frac{2 f_{gen} \cdot |P_{work}| \cdot t}{10^6},$$

where N_1 and N_2 are the numbers of frequency cycles per time t at f_1 and f_2, respectively. Time shift corresponding to $|N_1 - N_2|$ is calculated as:

$$\Delta t = |N_2 - N_1| \cdot T_{gen} = \frac{2 f_{gen} \cdot |P_{work}| \cdot t \cdot T_{gen}}{10^6} = \frac{2t \cdot |P_{work}|}{10^6}. \tag{5}$$

By rewriting expression (5) and substituting $\Delta t^{\max}$ in it, we get the maximum generator frequency correction period $T_{corr}^{\max}$:

$$T_{corr}^{\max} = \frac{\Delta t^{\max} \cdot 10^6}{2 \cdot |P_{work}|} = \frac{100 \cdot 10^{-12} \cdot 10^6}{\pm 0.6 \cdot 10^{-3}} \approx 0.167 \text{ c}.$$

According to the calculated value of $T_{corr}^{\max}$, synchronization sequence repetition period $T_{rep} = 3.2\,\text{ms}$ and frequency correction period $T_{corr} = 50\,\text{ms}$ were selected. Then according to expression (5), we get the maximum time shift between receiver and transmitter reference frequency cycles $\Delta t_{gen}^{\max}$ with typical reference oscillator instability P_{work} per time T_{corr} between the nearest corrections:

$$\Delta t_{gen}^{\max} = \frac{2 \cdot T_{corr} \cdot |P_{work}|}{10^6} = \frac{2 \cdot 50 \cdot 10^{-3} \cdot 0.3 \cdot 10^{-3}}{10^6} = 30\,\text{ps}. \quad (6)$$

To determine the required accuracy of the synchronization algorithm, it should be taken into account that signals in real digital circuits differ from ideal ones by the presence of jitter — undesirable phase or frequency deviations introducing additional error to the comparison of time windows on the receiver and transmitter. The amount of jitter is defined by parameters of the employed hardware components and doesn't depend on the quality of receiver and transmitter frequency synchronization. Therefore, the maximum allowable time shift between the generator cycles $\Delta t^{\max}$ during the correction period is calculated as:

$$\Delta t^{\max} = \Delta t_{sync}^{\max} + \Delta t_{jitter}^{\max} + \Delta t_{gen}^{\max},$$

where $\Delta t_{sync}^{\max}$ is the maximum time shift between reference oscillator cycles driven by the synchronization algorithm accuracy, and $\Delta t_{jitter}^{\max}$ is the maximum total jitter of receiver and transmitter working signals. It follows from expressions (6) and (7) that the maximum error of phase alignment at each synchronization algorithm iteration taking into account the jitter $\Delta t_{sync+jitter}^{\max} = \Delta t_{sync}^{\max} + \Delta t_{jitter}^{\max}$ is 70 ps ($\Delta t_{sync+jitter}^{\max} = 100 - 30 = 70\,\text{ps}$).

Since compensation of the generator frequency difference caused by Δf_{def} and Δf_{res} is necessary only when the QKD device is started, the frequency difference compensation procedure was divided into two stages. The first stage (starting correction), which is performed once, involves the compensation of Δf_{def} and Δf_{res}. The second stage (periodic compensation) is performed after each T_{corr} and is aimed at the compensation of P_{work} with accuracy satisfying the set maximum value of $\Delta t_{sync+jitter}^{\max}$.

Frequency correction at both stages is carried out by tuning the reference frequency f_{ref} of the receiver synthesizer. Since the receiver and transmitter synthesizer settings are identical, reference frequency synchronization will ensure synchronization of synthesized frequencies. For the Si5340 synthesizer, $f_{\text{ref}} = 200\,\text{MHz}$, used in the device, tuning to the target frequency is performed in accordance with the documentation of Si5340 and no additional calibrations are required. This approach is used to limit the maximum value of $\Delta f_{def} + \Delta f_{res}$ by the range of f_{ref} of the frequency synthesizer.

Note that in case of direct reference oscillator frequency variation by varying its control voltage, generator DAC shall be calibrated for tuning to the target frequency. Besides the required calibration and the presence of error introduced by DAC, a very small frequency tuning range ($\pm 3\,\text{Hz}$) compared with the range available on the Si5340 synthesizer ($\pm 3\,\text{Hz}$) is a big disadvantage of using reference oscillator for frequency correction. This disadvantage is critical because situations may occur where reference oscillator frequency ranges of the receiver and transmitter don't overlap. In this case, device operation becomes impossible without replacement of one of the reference oscillators, and the frequency range of the new reference oscillator shall be selected accordingly.

2.1. Starting frequency difference correction

Let's consider both stages one after the other. At the first stage, the current frequency difference is calculated by measuring the time T_{360} between two neighboring events of generator phase divergence of the receiver $\varphi_1(t)$ and transmitter $\varphi_2(t)$ by 360°. For this, the transmitter continuously sends synchronization pulses at $f_1^{initial}$ during time τ, and the secret key is not generated during the first frequency correction stage (the causes are described in Section 1). The receiver in turn uses $f_2^{initial}$ for measuring T_{360}. The receiver and transmitter phase difference $\Delta\varphi(t)$ is calculated as:

$$\Delta\varphi(t) = |\varphi_2(t) - \varphi_1(t)| = 2\pi|f_2^{initial} - f_1^{initial}|t.$$

For $\Delta\varphi(T_{360}) = 2\pi$ from the expression (8) we get

$$T_{360} = \frac{1}{|f_2^{initial} - f_1^{initial}|}.$$

Since the appearance of an extra cycle at the leading reference oscillator frequency corresponds to the time of phase divergence by 360°, these events can be easily recorded using digital technology, in particular, on FPGA, and T_{360} will be expressed in the number of cycles N_{360} of the sampling frequency f_m (with period T_m), at which the measurement is performed:

$$T_{360} = N_{360} \cdot T_m.$$

Then the current generator frequency difference Δf_{curr} can be expressed as:

$$\Delta f_{curr} = |f_2^{initial} - f_1^{initial}| = \frac{1}{N_{360} \cdot T_m} = \frac{f_m}{N_{360}}.$$

Note that for correct measurement of T_{360}, f_m shall satisfy $f_m > 2|f_2^{initial} - f_1^{initial}|$ in accordance with the Kotelnikov theorem. In particular case, when the same frequency as for generator phase difference analysis ($f_m = f_2^{initial}$) is used as f_m, taking into account equation (3), expression (9) is reduced to:

$$N_{360} = \frac{1 + |P_{work}| \cdot 10^{-6} + \frac{\Delta f_{\text{const}}}{f^{initial}}}{2|P_{work}| \cdot 10^{-6} + \frac{\Delta f_{\text{const}}}{f^{initial}}},$$

where $f^{initial}$ is the nominal frequency for $f_1^{initial}$ and $f_2^{initial}$. Since P_{work} and $\Delta f_{\text{const}}/f^{initial}$ are constant for all frequencies obtained by multiplying or dividing the synthesizer reference frequency f_{ref}, it follows from expression (10) that, when $f_m = f_2^{initial}$, N_{360} is also constant for this set of frequencies. Consequently, N_{360} calculated at $f_2^{initial}$ ($f_{ref} \neq f^{initial}$) may be used for calculating the current reference frequency difference of the receiver and transmitter by substituting the corresponding values into expression (9). So, our synchronization system uses $f^{initial} = f_{prep}/2 = 156.25$ MHz. This property also may be very helpful for reducing the evaluation time τ when using relatively low values of f_{ref} ($\tau \geq T_{360}$).

For implementing the N_{360} measurement mechanism, FPGA uses an algorithm for analysis of „empty“ signals generated by two FIFO (First In First Out) buffers with asynchronous read and write domains [26–28]. FIFO buffers are the hardware-software implementation of the „queue“ data structure in FPGA. „Empty“ signals are generally formed at the buffer reading frequency when there is no readable data in the buffer. In the FIFO implementation used in our QKD devices, this flag is activated at the beginning of the frequency cycle corresponding to reading the last available word in FIFO. After writing at least one word in FIFO, the „empty“ flag is deactivated indicating that data is now readable, but reading is resumed with a delay equal to one reading frequency cycle. In the proposed algorithm, FIFO inputs are configured as follows:

- FIFO 1: reading is performed at the receiver frequency, writing is performed at the transmitter frequency;
- FIFO 2: reading is performed at the transmitter frequency, writing is performed at the receiver frequency;

In case when reading and writing frequencies ($f_1^{initial}$ and $f_2^{initial}$) ideally coincide, the amount of data in buffers will be constant because one writing frequency cycle will correspond to each data reading frequency cycle, and „empty“ signals will not be generated in any of the buffers. Otherwise, in one of the used FIFO, the reading frequency will have a lead over the writing frequency, while reduction of the amount of data in the buffer will correspond to the appearance of every extra frequency cycle at the reading frequency. Regardless of the number of words in this buffer at the initial time, when the number of words in the buffer reaches 1, „empty“ signals will start to be generated. In addition, due to the FIFO read lock, the „empty“ signal appearance period measured at the receiver's internal frequency $f_2^{initial}$ will correspond to the current value of T_{360}. The leading frequency and, respectively, the receiver frequency tuning sign are unambiguously defined by the frequency, at which reading takes place from the buffer that generates „empty“ signals.

Note that the measurement starting time of N_{360} randomly relates to the current reference oscillator phases, therefore, to unambiguously determine N_{360}, at least two events of reference oscillator phase difference by 360° during the evaluation time τ should be recorded. In terms of FPGA, this condition is satisfied by choosing the highest from the derived estimates of N_{360}, and by measuring the number of „empty“ events per τ: when the number of „empty“ events is less than 2, the procedure is performed again with the increased evaluation time τ.

Since the minimum time required to correctly evaluate T_{360} corresponds to the current frequency difference period ΔT_{curr}, the first correction stage for the current reference oscillator frequencies may require longer time, and in the limiting case τ tends to infinity. To reduce τ, the proposed starting frequency correction system uses the method of artificial increase of Δf_{curr} to values significantly exceeding Δf_{work} by creating the intentional frequency difference Δf_{const} (expression (3)).

2.2. Periodic frequency difference correction

As mentioned above, the frequency difference correction algorithm during device operation is based on the periodic correction of the receiver synthesizer reference frequency f_{ref} in accordance with the transmitter reference oscillator frequency drift. A common approach to solution of this problem is to use a phase-locked loop (PLL) in periodic mode [29–31]. Generally, PLL is a control system using a negative feedback loop for phase and frequency synchronization of the master and slave generators. Phase detector, which performs generator phase comparison and error signal generation proportionally to the current phase difference, is the main component of this system. In classical PLL systems, the received error signal is supplied via the low frequency filter to the voltage-controlled oscillator (VCO) control input, thus correcting the generator frequency and maintaining the constant phase difference. Phase locking quality depends on many parameters such as phase detector accuracy and generator control accuracy.

Our synchronization system uses a FPGA-based hardware phase detector consisting of a multiplexer, D flip-flop and a set of auxiliary registers [32]. RTL circuit diagram of the D flip-flop and multiplexer is shown in Figure 2: a signal from the synchronizing detector (tx_clock) is sent to the synchronization input C of the D flip-flop, a signal from the multiplexer is sent to data input D. The multiplexer is operated using the receiver's 156.25 MHz internal signal

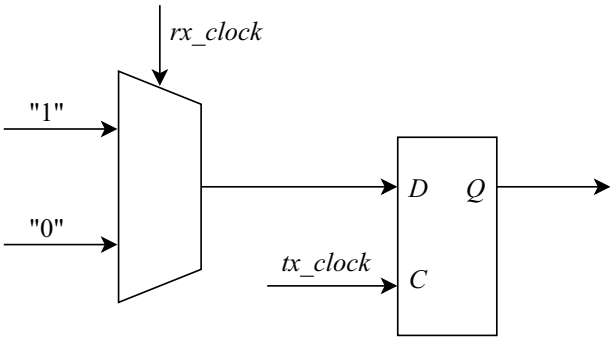

Figure 2. RTL-circuit diagram of the D flip-flop and phase detector multiplexer.

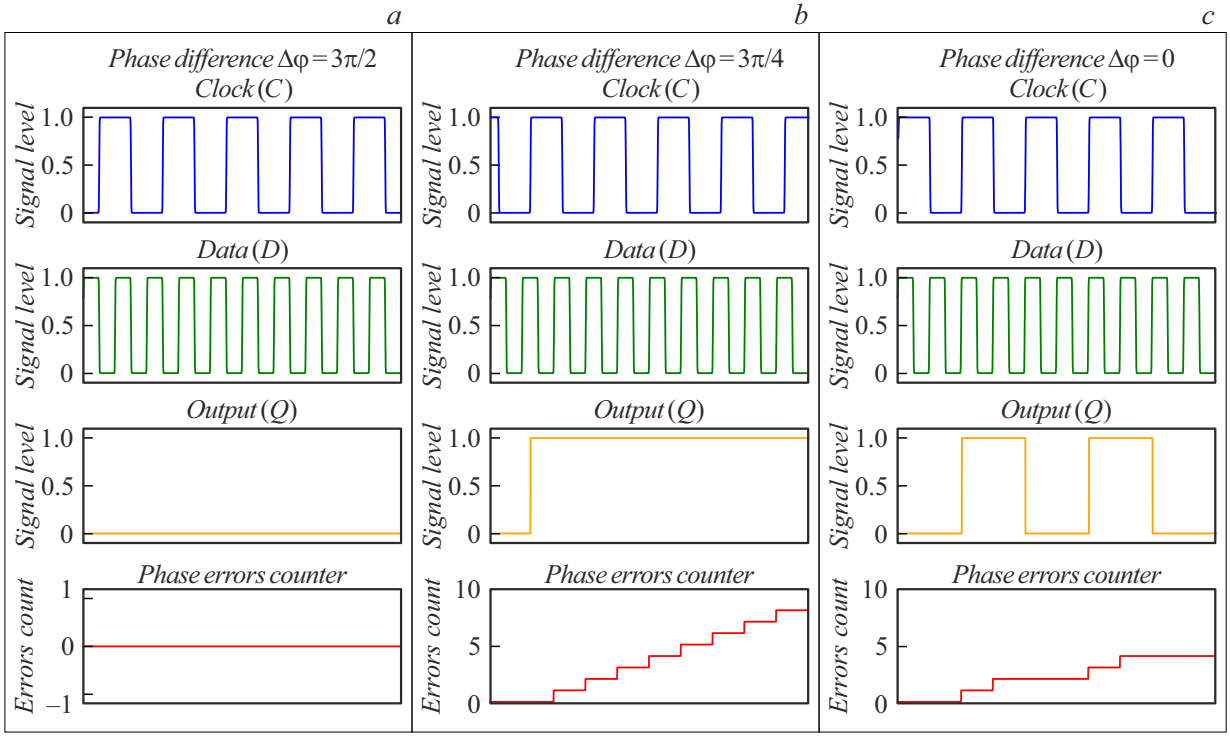

Figure 3. Simulation of phase detector operation depending on the phase difference $\Delta\varphi$ between the analyzed signals at the D flip-flop inputs.

(rx_clock) with logic 1 formed at the multiplexer output when the control signal is also equal to logic 1. A synchronization detector signal carrying the information about the master generator frequency is formed using the synchronization sequence with a fixed length sent by the transmitter with $T_{rep} = 3.2$ ms.

For each synchronization sequence pulse, a signal representing a phase error of this pulse is generated at output Q of the D flip-flop: if the positive front of the clock pulse arrives at the flip-flop at the time when the receiver's internal frequency is equal to logic 1, logic 1 corresponding to the existing phase error will be also formed at output Q, otherwise logic 0 will be formed.

Then the sum of received signals for all synchronization sequence pulses — accumulated phase error is used as a total error signal of the phase detector. Accumulated phase error is calculated by the positive front of a signal sent to data input D during the time defined by the phase error calculation window time. Owing to the calculation window, the effect of other synchronization sequence segments and noise in the quantum channel on the accumulated phase error is avoided (final synchronization sequence configuration is discussed in Section 3).

It is known that two time requirements shall be met for proper operation of any flip-flop: signal setup time and hold time at input D [33–35]. However, phase difference between the receiver signal and synchronization sequence is generally random, therefore the mentioned-above time requirements will be not be always met inducing a flip-flop metastability phenomenon. Therefore, to avoid transition of the level of output Q to the intermediate state, our circuit uses the multiplexer signal, rather than directly the receiver operating frequency, as a signal for input D. Due to metastability, the proposed phase detector implementation may have three different states:

- arrival time of all synchronization pulse fronts corresponds to the absence of pulses at the receiver frequency: the accumulated phase error is equal to 0 (Figure 3, *a*);
- arrival time of all synchronization pulse fronts corresponds to the presence of pulses at the receiver frequency: the accumulated phase error is maximum (Figure 3, *a*);
- arrival time of synchronization pulse fronts is close to pulse fronts at the receiver frequency: due to the presence of signal jitter and metastability phenomenon, the accumulated phase error has an intermediate value, a smooth transition between the minimum and maximum phase error occurs (Figure 3, *c*).

Besides the transition process, it shall be also taken into account that there is an additional uncertainty source of accumulated phase error caused by the fact that different frequencies: receiver and transmitter, are used for phase error signal registration and generation. Therefore, loss of information about phase errors is possible depending on the relation of these frequencies and the current phase difference between them. To remove this instability source, our circuit uses 78.125 MHz for generation of periodic synchronization sequence. In this case, two fronts at 156.25 MHz will correspond to each phase error pulse,

which ensures reliable recording of each error. In this case, the maximum accumulated phase error will correspond to the doubled synchronization pulse count used for phase error calculation.

Since the intermediate value of phase error unambiguously defines the relative positions of the signal fronts, this property can be used for frequency difference correction of these signals. For this, it is sufficient to keep the value of the phase error in the chosen intermediate position by smooth tuning of the receiver synthesizer reference frequency f_{ref}. For this, our feedback loop uses a proportional-derivative (PD) controller, whose output signal is a final feedback signal [36,37]. The objective of this controller at each algorithm iteration is to maintain the constant phase difference of the reference frequencies of the receiver and transmitter synthesizers by correcting the current reference frequency of the receiver synthesizer. New value of $f_{ref}(n)$ is calculated as follows:

$$f_{ref}(n) = f_{ref}(n-1) - (P + D),$$

where P and D are proportional and differentiating components, respectively, $f_{ref}(n-1)$ is the synthesizer reference frequency at the previous frequency correction iteration. Controller components are calculated as follows:

$$P = K_p \cdot (e(n) - \Delta e_{\text{const}}),$$

$$D = K_d \cdot (e(n) - e(n-1)),$$

where K_p and K_d are proportional and differential component coefficients, respectively, $e(n)$ and $e(n-1)$ are phase errors at the current and previous algorithm iterations, respectively, Δe_{const} is the target value of phase error. From expressions (11)–(13), it follows that K_p and K_d, and Δe_{const} are the parameters of the proposed periodic frequency difference correction system. Accordingly, system configuration reduces to determining the parameter values at which the actual synchronization accuracy will satisfy the threshold value. $\Delta t^{\max}_{sync+jitter} = 70$ ps [38].

3. Method for alignment of optical pulse reception and transmission start times on each node

As described in Section 1, we use the time division multiplexing method to send synchronization sequences via the quantum channel. Durations of both sequence sending time windows and delays between them expressed in the number of 156.25 MHz frequency cycles are set to the same values on the receiver and transmitter. Thus, full duration of one iteration of data exchange cycle between nodes is determined. Consequently, besides the compensation of reference oscillator frequency difference, procedure of determining the start time of next data exchange cycle iteration on the receiver with respect to the start time on the transmitter shall be performed regularly. Otherwise, situations may occur where the receiver will not receive signal qubits because they will arrive at the time corresponding to the synchronization sequence reception window. Note that this effect will also occur, if the time window durations or arrangements on nodes are different.

The proposed method performs transmission of information about the start of new cycle iteration on the transmitter by including one period of a 127 bit M sequence encoded in the form of optical pulses at the end of the synchronizing sequence. M sequence is a pseudorandom binary sequence obtained using a linear feedback shift register (LFSR) [39]. The primitive polynomial $P(x) = 1 + c_3x^3 + c_7x^7$ was used for sequence generation. Key property of the M sequence s is its correlation property [40,41], according to which unnormalized ACF R for shift n is calculated as:

$$R(n) = \sum_{m=1}^{N} s[m] \cdot s[m+n] = \begin{cases} N & \text{if } n = 0 \\ -1 & \text{if } 0 < n < N. \end{cases} \quad (14)$$

Expression (14) is true for the M sequence where all bits equal to 0 are converted to bits with the value -1. As can be seen from (14), with sufficient length of the M sequence, $R(0)$ is much higher than other ACF values, due to which noise-resistance and detection ability of M sequences grow significantly [42].

To determine the quantum state reception start time, the receiver performs continuous calculation of the unnormalized ACF of its transmitter M sequence copy and the received synchronization sequence in the corresponding time window. At the time when the analyzed sequences overlap, the receiver will receive the ACF peak with high signal-to-noise ratio. Reference frequency cycle number corresponding to the received ACF peak will correspond to the completion time of M sequence generation on the transmitter. Consequently, using the same frequency cycle count as the transmitter for delay after M sequence completion, the receiver will receive the reference frequency cycle number corresponding to the arrival of the first quantum state taking into account the delay in the quantum channel.

ACF is calculated by the correlator on FPGA using the bitwise multiplication, followed by summation of all bits of the resulting sequence. The received ACF value is compared with the set threshold value of R_{th}, which serves as the ACF peak detection criterion. Since the components of used M sequence can take the values of 0 and 1, and there are one more 1s than 0s, the maximum value of ACF $R(0)_{\max}$ is calculated as:

$$R(0)_{\max} = \lceil L_s/2 \rceil = \lceil 127/2 \rceil = 64.$$

Using $R_{\text{th}} < R(0)_{\max}$, we can compensate the effect of distortions in the recorded M sequence. Non-ideal setting and functioning of the synchronization laser and detector described in Section 1 may serve as distortion sources in this case. Note that optical fiber has constant level of loss and is not the source of noise in the M sequence.

Schematic diagram of the final synchronization sequence configuration formed by the transmitter after completion of

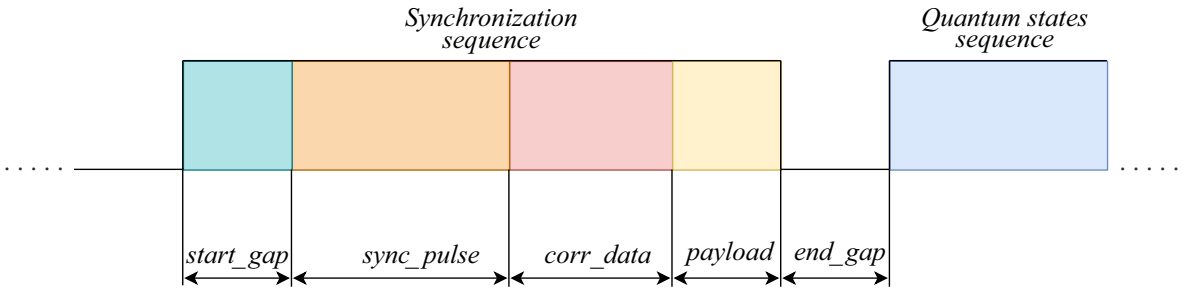

Figure 4. Schematic diagram of the used synchronization sequence configuration.

the first frequency difference evaluation stage is shown in Figure 4. The „sync_pulse“ segment corresponds to the periodic 78.125 MHz pulse sequence used in the frequency correction procedure described in Section 2.2. The receiver knows the pulse count formed by the transmitter on the „sync_pulse“ segment and uses this information to determine the phase error calculation completion time. Then on the „corr_data“ segment at 156.25 MHz, the M sequence is transmitted. Choice of different frequencies for various segments is necessary because in case of bitwise multiplication of the periodic 156.25 MHz pulse sequence by the 156.25 MHz M sequence copy, the resultant sequence will be equal to the used M sequence. Consequently, the value of ACF $R = R(0)_{\max}$ exceeding the threshold value R_{th} will be obtained. This will result in erroneous recording of the M sequence followed by misalignment of the reception and transmission window start times.

Delay corresponding to the „start_gap“ segment is necessary because the first laser pulses in the synchronization sequence are instable and can affect the phase error evaluation procedure. Instability of these pulses is associated with transition processes occurring during synchronization laser ignition. The „payload“ segment is used to send payload, in this case — the current iteration number of the key distribution cycle. The „end_gap“ segment is used as a delay before the start of signal quantum state reception window and is necessary to minimize the effect of residual reflections of the synchronization sequence in the quantum channel on single photon detectors.

4. Experimental Section

For experimental testing of the proposed synchronization system, all system components, including the optical scheme and control algorithms, were integrated in our BB84 QKD device. Fine tuning of the synchronization laser module, synchronization detector and variable optical attenuator VOA2 (Figure 1) provided stable registration of optical pulses in the SMF-28e optical fiber length range from 0 km to 125 km between the receiver and transmitter, and synchronization system correction for various lengths was performed only using the VOA2 attenuator. So, Figure 5, *a* shows the waveform of the synchronization sequence recorded at 100 km of the SMF-28e optical fiber. In particular, Figure 5, *b* and *c* shows segments corresponding to the synchronization sequence for phase error and M sequence calculation, respectively. It can be seen that the used laser pulse repetition frequency is twice as small, and the pulse shape in Figure 5, *b* is no different from the shape in Figure 5, *c*, which is indicative of correct operation of the synchronization detector at the given optical line length.

Then, we tested the proposed phase detector implementation. As shown in Section 2.2, operation of the periodic frequency correction algorithm is based on using the transient process in the value of phase error to maintain constant phase difference between the receiver and transmitter reference oscillator. To confirm the appearance of this process, the accumulated phase error was measured depending on the phase difference between the 5 000-pulse long synchronization sequence and the 78.125 MHz receiver signal. Frequency difference correction was not performed during the experiment. The measurements are shown in Figure 6. It can be seen that the obtained dependence coincides with the simulation results shown in Figure 3. Thus, it follows from Figure 6, *a* that the accumulated phase error is a periodic function, and the maximum phase error is 10 000, which corresponds to a doubled length of the used synchronization sequence. Figure 6, *b* demonstrates that there is a transient process, whose parameters depend on the frequency difference of measured signals during measurement.

Since the proposed frequency difference start correction system doesn't require additional adjustment (Section 2.1), the final system adjustment step is the determination of parameters of the PD controller used for the periodic correction (Section 2.2). For this, we used an empirical tuning method, during which various parameter combinations were tested [38]. Note that all subsequent measurements were performed with the same PD controller parameters.

After completion of setup for quantitative evaluation of the proposed synchronization system, we performed a set of experiments, during which a delay between Alice's and Bob's 156.25 MHz signals were studied at various optical line lengths in periodic frequency correction system operation. These signals were directly sent to the measuring equipment from the test SMA outputs on the FPGA

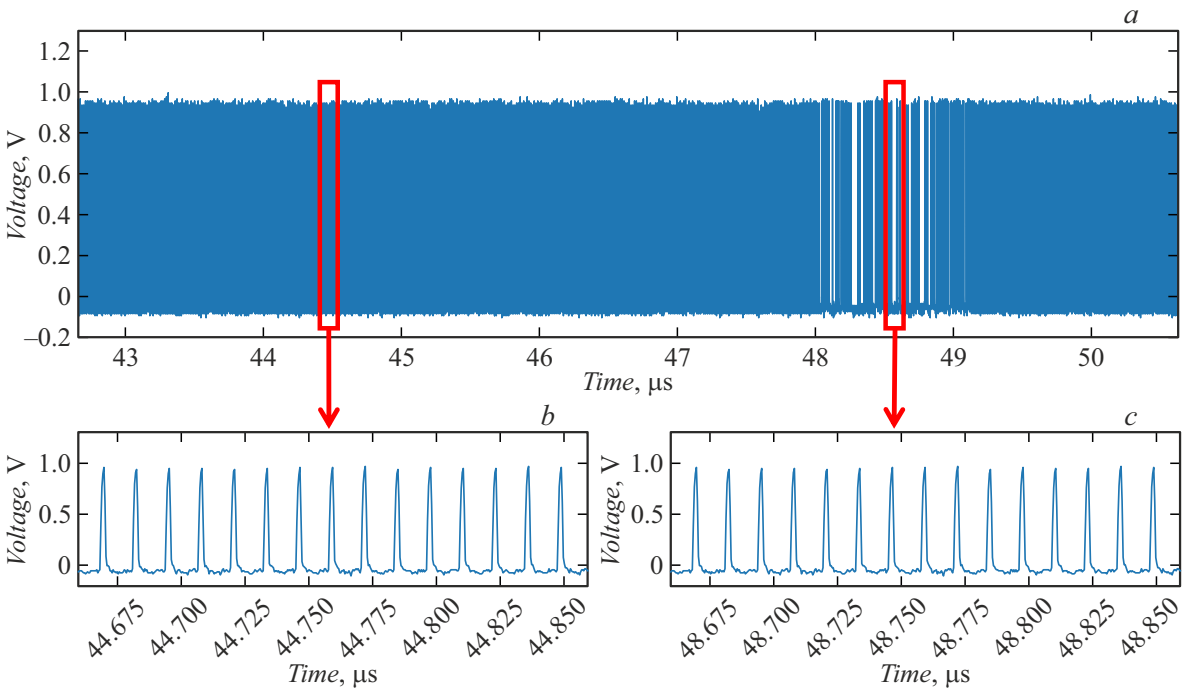

Figure 5. Waveform of the employed synchronization sequence configuration.

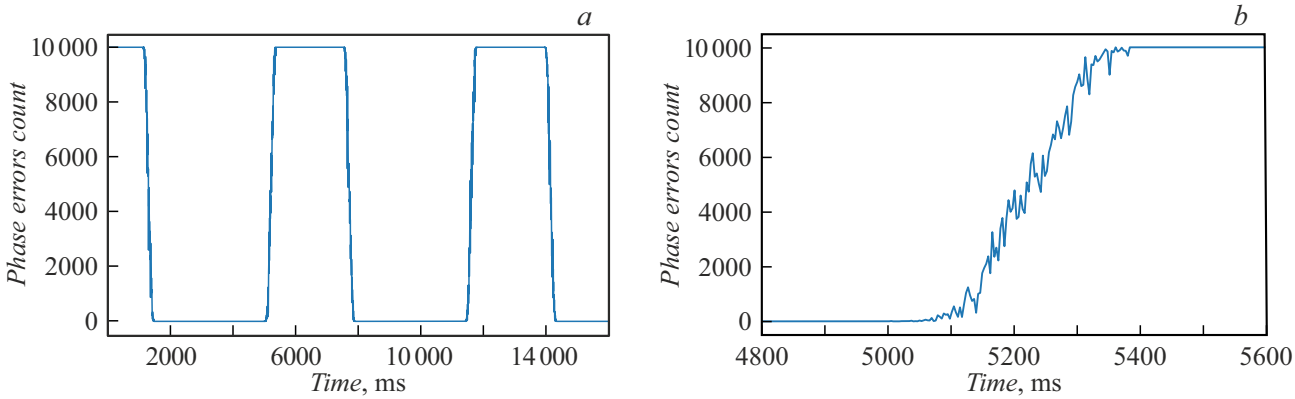

Figure 6. Experimental measurements of the accumulated phase error at the phase detector output.

board. The first experiments used the Teledyne LeCroy WaveRunner 8404m oscilloscope with a sampling rate of 40 Gs/s for correct evaluation of delay. Histograms of the measurement results for 0 km and 100 km optical line are shown in Figure 7; unbiased estimates of the standard deviation σ_{sum}^{meas} (SD) for these distributions are given in Table 1. The shape of the obtained distributions indicates that the proposed synchronization system works correctly to maintain the constant phase difference of synthesizer reference frequencies. The SD value obtained from these distributions makes it possible to estimate the overall timing accuracy between the receiver and transmitter as it incorporates the contribution of several components simultaneously:

$$\sigma_{sum}^{meas} = \sqrt{\sigma_{sync}^2 + \sigma_{gen}^2 + 2\sigma_{jitter}^2 + \sigma_{osc}^2},$$

where σ_{sync} is SD determined by the frequency correction accuracy, σ_{gen} is SD caused by reference oscillator frequency drift over the adjustment period, σ_{jitter} is SD of the measured signal jitter, σ_{osc} is SD of the oscilloscope time jitter used for the measurements. According to the documentation for the used oscilloscope, $\sigma_{osc} = 4$ ps. As mentioned earlier, control signal jitter affects not only the measurement results but also the overall correct synchronization ability, and the σ_{jitter} must be be taken into account twice, since the receiver and transmitter jitters are independent of each other.

Since the obtained distribution shape is close to normal, we use the three-sigma rule to evaluate the achieved synchronization accuracy. For this, consider the previously selected values $\Delta t^{\max} = 100$ ps, $\Delta t_{gen}^{\max} = 30$ ps and $\Delta t_{sync+jitter}^{\max} = 70$ ps as limits of the corresponding ranges

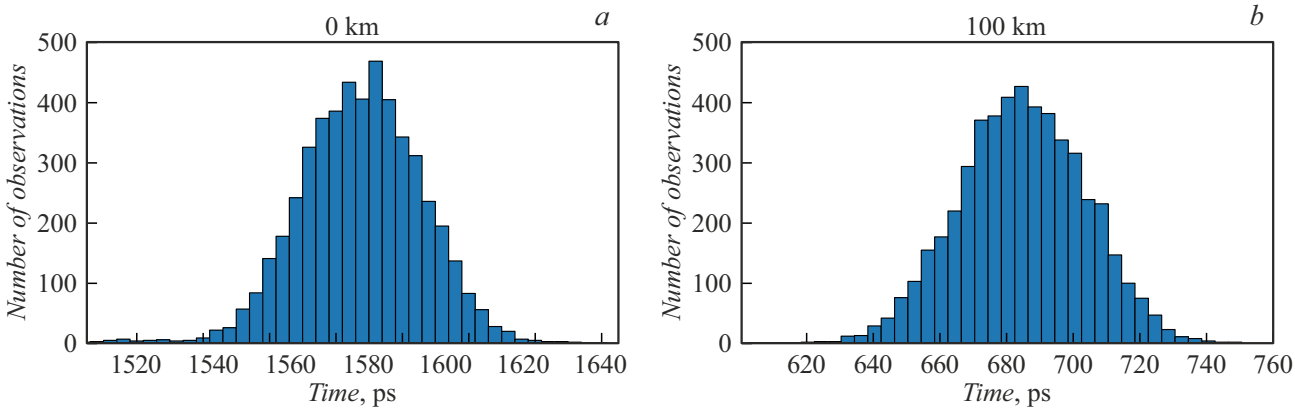

Figure 7. Distribution of delay between the receiver and transmitter operating frequency front at 0 km and 100 km of optical fiber.

Unbiased estimates of the total standard deviation of delay at various optical line lengths

Optical line length, km	$\sigma_{\text{sum}}^{\text{meas}}$, ps	σ_{sum}, ps	$\sigma_{\text{sync+jitter}}$, ps
0	≈ 18.5	≈ 18.07	≈ 15.05
100	≈ 18.88	≈ 18.45	≈ 15.5

$(\mu - 3\sigma; \mu + 3\sigma)$. μ is a mean time shift between the receiver and transmitter reference frequency cycles and may be omitted in further discussion ($\mu = 0$). Then, using $\Delta t^{\max} = 3\sigma^{\max}$, we get the following relation for the delay SD without considering the oscilloscope jitter σ_{sum}:

$$3\sigma_{sum} \in (-\Delta t^{\max}; \Delta t^{\max}). \qquad (16)$$

Similarly, for the delay SD without considering the oscilloscope jitter and receiver and transmitter reference oscillator frequency drift $\sigma_{sync+jitter}$, using $\Delta t_{sync+jitter}^{\max} = 3\sigma_{sync+jitter}^{\max}$, we get:

$$3\sigma_{sync+jitter} \in (-\Delta t_{sync+jitter}^{\max}; \Delta t_{sync+jitter}^{\max}), \qquad (17)$$

Table 1 shows the synchronization accuracy estimates calculated using expression (15). These estimates suggest that the achieved synchronization accuracy on both optical lines satisfies the synchronization system requirements stated in conditions (16) and (17) ($3\sigma_{sum} < 100$ and $3\sigma_{sync+jitter} < 70$ ps). It should be noted that in Section 2 it was shown that fulfilling these requirements provides sufficient synchronization accuracy for our QKD device within one frequency correction period ($T_{corr} = 50$ ms).

Then, to confirm correct system operation at long time intervals, synchronization stability at long time intervals was studied. For this, distribution of delay between Alice's and Bob's signals were measured at the given time interval, similar to the measurements from the previous experiment. For the purpose of experiment automation, the Swabian Time Tagger 20 streaming time-to-digital converter with the specified time jitter RMSD of 34 ps was used instead of an oscilloscope. During the experiment, the frequency correction system worked in periodic mode, measurements were carried out every 5 min using the converter time window width of 10 ps, statistics were collected during 10 s.

Figure 8 shows the results of two experiments obtained using two independent QKD devices and optical lines 0 km and 100 km in length, respectively. As shown in the diagrams, delay SDs remained constant throughout the experiment with minor fluctuations, which didn't affect the QKD device operation. The observed difference in the fluctuation amplitudes of the SD for the two QKD devices is caused by the individual characteristics of the optical synchronization scheme components, in particular, the parameters and stability of the synchronization lasers and synchronization detectors (the PD controller parameters in both devices were the same). The findings suggest that the proposed frequency difference correction system has high time stability on optical lines of various lengths. Note that the difference between the SD values shown in Figure 8 and those in Table 1 results from large measurement error of the Swabian Time Tagger 20.

The next stage involved a study performed to demonstrate correct operation of the proposed system for optical pulse reception and transmission start time alignment. Figure 9 shows the waveforms demonstrating relative positions of the quantum state receiving and transmitting windows on Alice and Bob for different optical lines. Synchronization sequence detecting results on the receiver were used as synchronization sequence waveforms. It can be seen that the synchronization sequence position coincides with intervals between the quantum state receiving windows, which confirms correct operation of the time division multiplexing system in the optical channel. As shown in the lower diagram in Figure 9, the receiving window time shift with respect to the transmitting window corresponds to the delay induced when the optical signal passes through the 100 km optical fiber. Therefore, it may be concluded that relative positions of the windows as shown in the upper and middle diagrams in Figure 9 provide correct registration

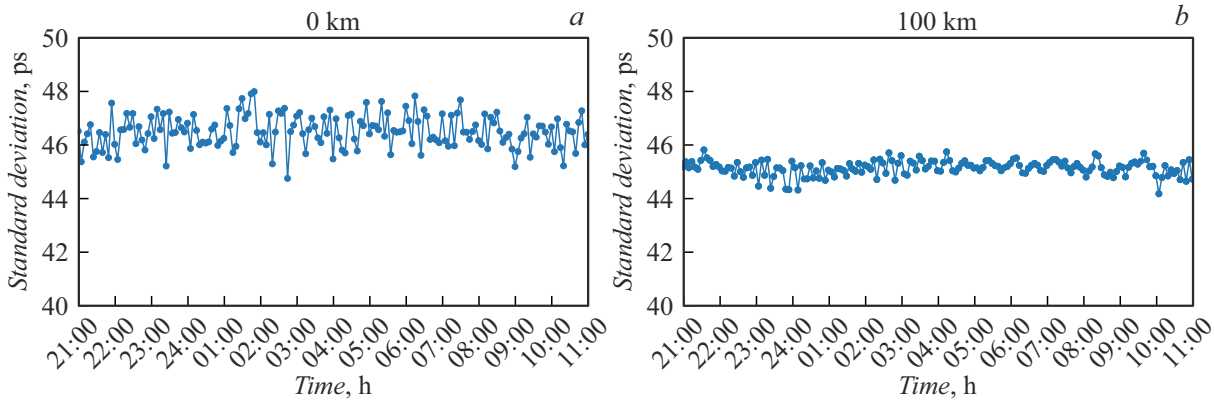

Figure 8. Unbiased SD estimate of the delay between receiver and transmitter signals at 156.25 MHz versus time for optical line lengths of 0 and 100 km.

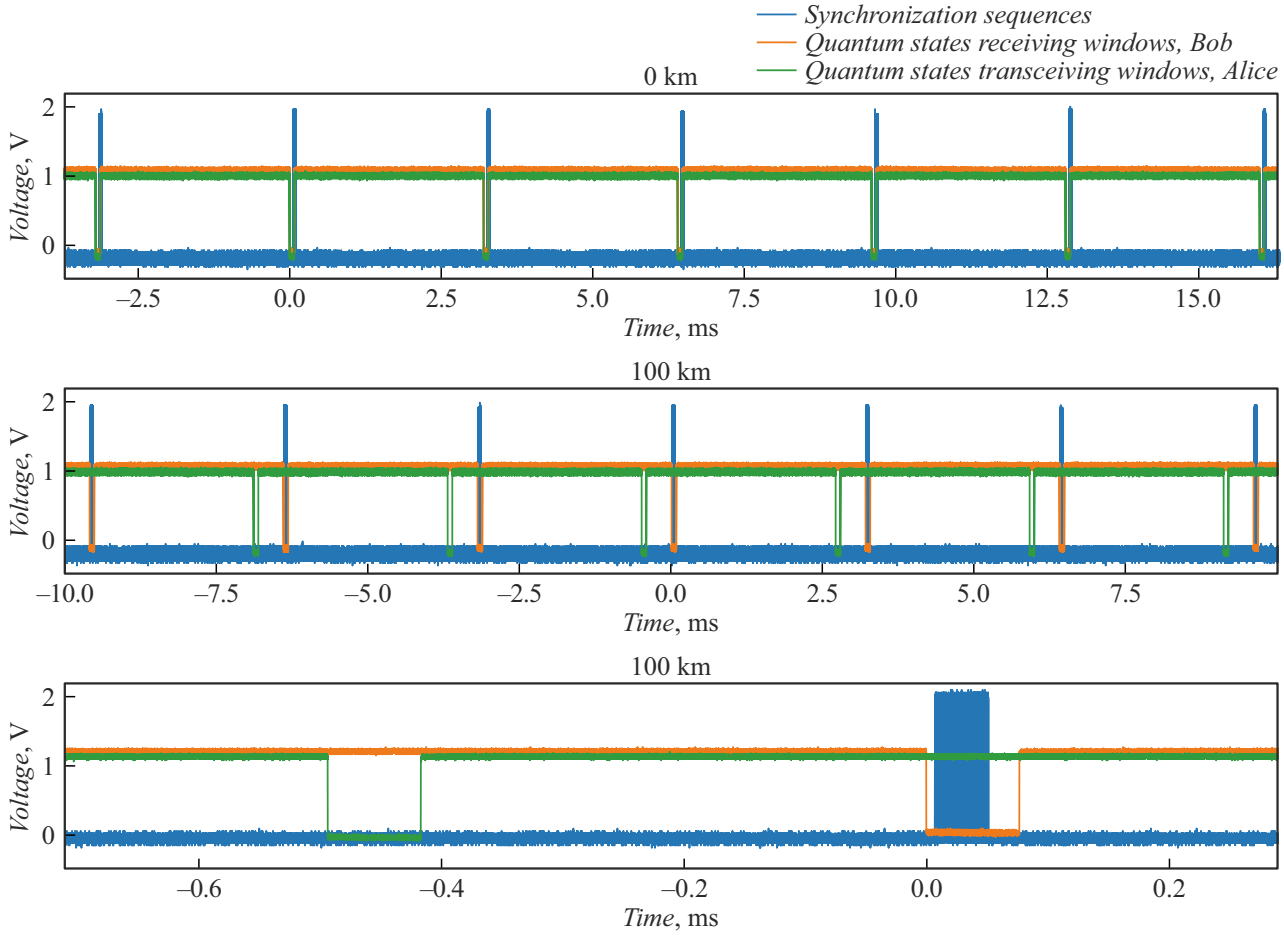

Figure 9. Waveform of quantum state receiving and transmitting windows and synchronization sequences between them.

of quantum states by the receiver taking into account the quantum channel delay.

Final testing of the developed synchronization system included a quantum key distribution session using a standard 25 km fiber-optic channel. Throughout the session, the sifting and secret key generation rate was ≈ 60 and ≈ 20 Kbit/s, respectively [22]. Key generation was never interrupted, which confirms the previous experimental results and suggests high stability of both the synchronization system and QKD device as a whole. Mean QBER level during the experiment was $\leq 4\%$. QBER monitoring results are shown in Figure 10 and indicate that the proposed system has good synchronization accuracy.

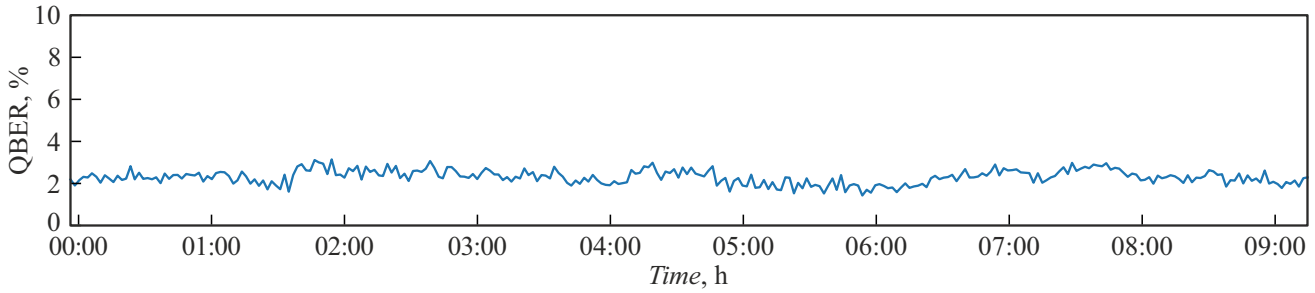

Figure 10. Dependence of QBER on time in quantum key generation mode using a 25 km quantum channel.

Conclusion

The paper examines in detail an implementation of generator frequency difference correction system for QKD devices. An optical synchronization scheme was proposed that uses time and frequency division multiplexing methods for signals, as well as an algorithm for its configuration, allowing for rapid adaptation to optical lines of various lengths. Moreover, stability parameters of reference oscillators used in the device were analyzed to formulate correction accuracy requirements. Based on the obtained results, a two-stage method was developed that ensures effective frequency difference correction during device operation, while the impact of the synchronization system on secret key generation was minimized. A noise-resistant method was also developed for automatic determination of the quantum state reception and transmission start times on the receiver and transmitter, respectively.

To validate the proposed hardware and software solutions, a series of experiments was carried out using a commercial QKD device implementing the BB84 protocol. As a result, it has been demonstrated that all components of the proposed frequency difference correction system operate stably with accuracy meeting the established requirements.

As potential areas for further evolution of the system, it is proposed to implement an automatic PD controller tuning algorithm to simplify the calibration process and increase synchronization stability under conditions of changing channel characteristics [38]. Significant upgrading of the components used in the optical scheme is also proposed. Thus, a wide dynamic range photodiode and automatic gain control (AGC), mechanism used as part of the synchronization detector will significantly improve the signal registration quality and general system reliability in heavy operating conditions [43]. Moreover, this will considerably simplify the adjustment procedure for the proposed optical scheme.

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Conflict of interest

The authors declare no conflict of interest.

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