Semiconductors, 2024, Vol. 58, No. 5

Reproducibility of the electrophysical characteristics of the prototype transistor structures based on the graphene–CaF_2–Si(111) heterosystem

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Received May 24, 2024
Revised June 7, 2024
Accepted July 7, 2024

Statistical distributions of the current have been studied for the set of the prototype transistor structures with a two-dimensional graphene film over the insulating calcium fluoride layer grown by molecular beam epitaxy. Such material combination is new for this field. The obtained characteristics were rather attractive, keeping the spread parameters (such as dispersion of the drain current or of the position of charge neutrality point at the current and voltage scale) within the tolerable limits. The studies in this area are important for development of „two-dimensional" electronics based on transistors whose prototype structures were under consideration in the work.

Keywords: 2D electronics, graphene, calcium fluoride, reliability.

DOI: 10.61011/SC.2024.05.59175.6719

1. Introduction

In short communication [1] we presented a device fabricated on the basis of an original combination of materials, — a Field-Effect-Transistor (FET) with two-dimensional (2D) current-conducting channel made of graphene (G) and with epitaxial calcium fluoride (CaF_2) acting as a gate insulator. The following characteristics of the transistor were given: $I_g(V_g)|_{V_d=\mathrm{const}}$, $I_d(V_g)|_{V_d=\mathrm{const}}$, $I_d(V_d)|_{V_g=\mathrm{const}}$ (legends: V — voltage, I — current, g — gate, d — drain), that proved the samples operability.

It should be emphasized that it is premature to treat the studied heterostructures as full-fledged transistors being practically introduced into microelectronics at this stage. More realistically, they should be considered as prototypes of future devices of this class.

However, even at the initial stage of the study of structures, information is needed about spread, reproducibility, and repeatability of curves. Without this information, we may only confirm the validity of the physical principle of operation, leaving aside the technical application-critical aspects. Therefore, in paper [2] we covered the topic of the characteristics variation for this class of prototypes, and in this paper, having studied a larger number (hundreds) of fabricated samples, we focus on statistical issues (statistics included all samples, rejection was not required). Presentation of the results is preceded by a short section describing the operation principle of GFET device with CaF_2 and justification of the problem relevancy in general.

2. Operation principle of GFET with CaF_2

Among the key tasks of microelectronics at the present — the search for new architectures and combinations of materials for fabrication of FET. One of the promising systems is a structure [3,4] with a 2D channel made of a material like molybdenum (or other transition metal) dichalcogenide, black phosphorus or graphene film. The channel (conducting film) is formed above the dielectric isolating it from the gate. With the change of the transverse field value the channel resistance becomes varied. Despite the fact that prototypes of such transistors appeared already in the mid 2010s, the problem of optimizing the choice of materials has not yet been solved either in relation to the channel or in terms of dielectric selection.

Possible design for that transistor is schematically shown in Figure 1. The backgate electrode with a voltage V_g here acts as a gate; it controls the value of current I_d from the source to drain. The most significant processes unfold in a conductive 2D layer deposited on top of the dielectric, unlike conventional transistors, where the channel is an inversion region in Si at the interface with the isolator. Although in real-life devices control should be performed „from the top", the backgate configuration, as a more simple version, can serve as a test for preliminary study of the properties of a heterostructure with a new combination of materials.

Graphene is potentially attractive due to high mobility of the charge carriers, while ultra-thin ($1-3$ nm) calcium fluoride is of interest due to a new progress in its growth technology and good dielectric properties (wide band gap $E_g = 12.1$ eV, high static permittivity 8.43, breakdown field $> 10^7$ V/cm etc. [5,6]).

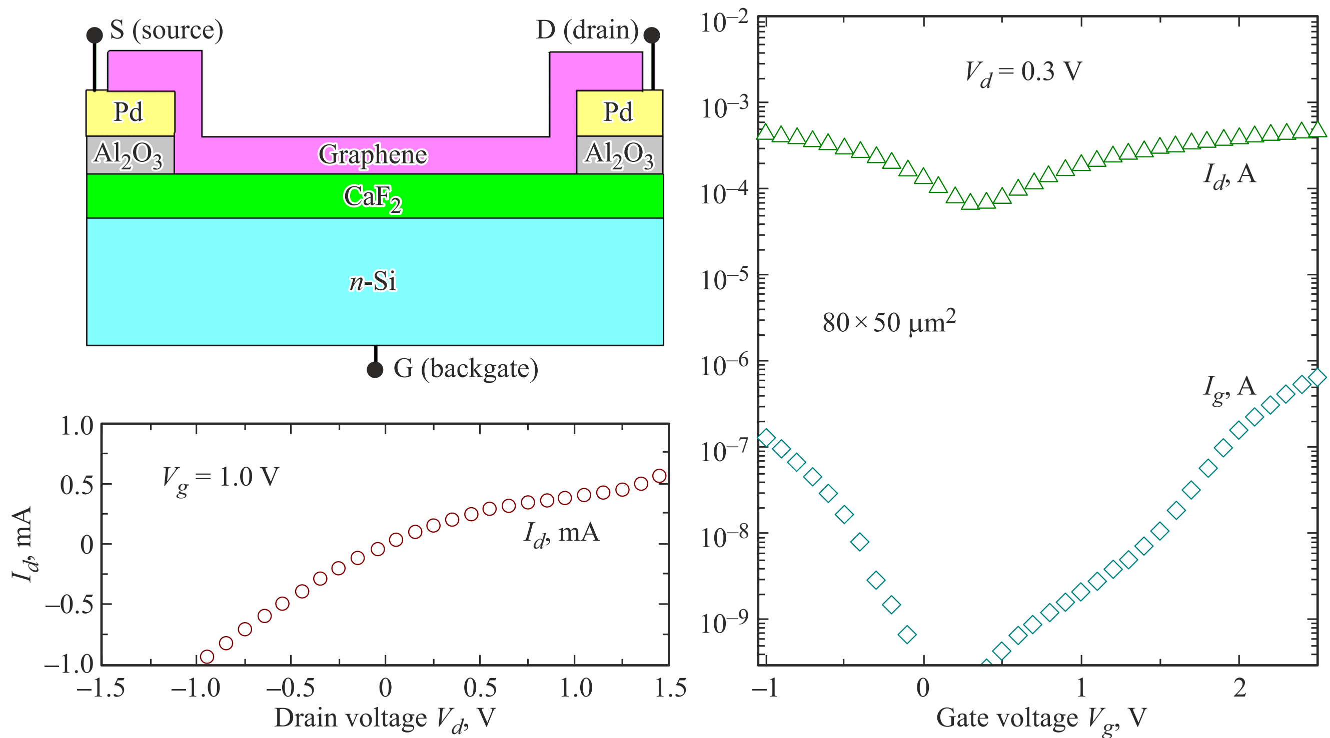

Figure 1. Studied heterostructure — transistor prototype (schematic view). Graphene film acts as a current-conducting channel, and fluoride — as a gate dielectric. Typical characteristics: drain current I_d and leakage current to gate I_g as a function of voltage V_g on gate with fixed drain voltage V_d, as well as I_d as a function V_d at given V_g (size of gate $80 \times 50\,\mu m^2$). (A color version of the figure is provided in the online version of the paper).

Figure 1 illustrates the data from paper [1] on characteristics of our fabricated structures of discussed type, which suggests their functionality and controllability. In particular, it is seen that the leakage current I_g is far lower than the main current I_d, while, as easily verified through the division by the area $L \times W$, the leakage current density is several orders lower than $1\,A/cm^2$. The sign of current I_d changes when crossing zero for the drain voltage V_d, and current I_d itself is expressly dependent on V_d and V_g, while the minimum of curve $I_d(V_g)$ is shifted to the right with the growth of positive voltage V_d.

At the qualitative level, the described behavior is typical for all measured samples, of which about one hundred were fabricated and studied.

3. CaF_2 layer growth technology

Since calcium fluoride is a very new material, and the presence of defects in it affects the stability of the devices specifications (undesirable charging phenomena may occur), it is useful to provide information about our technology for fabrication of thin films of CaF_2.

The layer of CaF_2 was formed by molecular-beam epitaxy (MBE) method on moderately doped substrates of n-type of Si ($N_D = 10^{15}-10^{17}\,cm^{-3}$) with orientation (111). After treatment by Shiraki method [7], according to which a thin layer of oxide was repeatedly chemically grown and removed, the finish layer of silicon oxide SiO_2 was thermally evaporated in conditions of superhigh vacuum, after which epitaxial growth of CaF_2 was started with a rate of $1-1.5$ nm/min. Growth temperature of 250°C without annealing turned out to be optimal. Crystalline quality was controlled by the reflection high-energy electron diffraction pattern (energy of 15 keV).

The regions of drain and source terminals were formed above CaF_2 with the use of photolithography: 10-nanometer sublayer of Al_2O_3 with palladium metallization. Commercial graphene film, several square centimeters in size, grown by chemical vapor deposition was transferred to the formed structure; polymethylmethacrylate was used during the transfer. The channel dimensions (length $L\times$ width W) were from $160 \times 100\,\mu m^2$ to $9 \times 3\,\mu m^2$, most of the measurements were made for devices $80 \times 50\,\mu m^2$. The applied scalable technology allowed simultaneously fabricating of up to a hundred of transistor structures graphene$-CaF_2-$Si. The electrical properties of graphene complied with today's standards.

Nominal thickness of fluoride d_n was $5-10$ nm, thickness deviation $\sim 0.5-1.1$ nm; 7-nanometer samples were taken for illustrations. These samples were fabricated in several processes identical in terms of their technological parameters; no difference was revealed between the structures

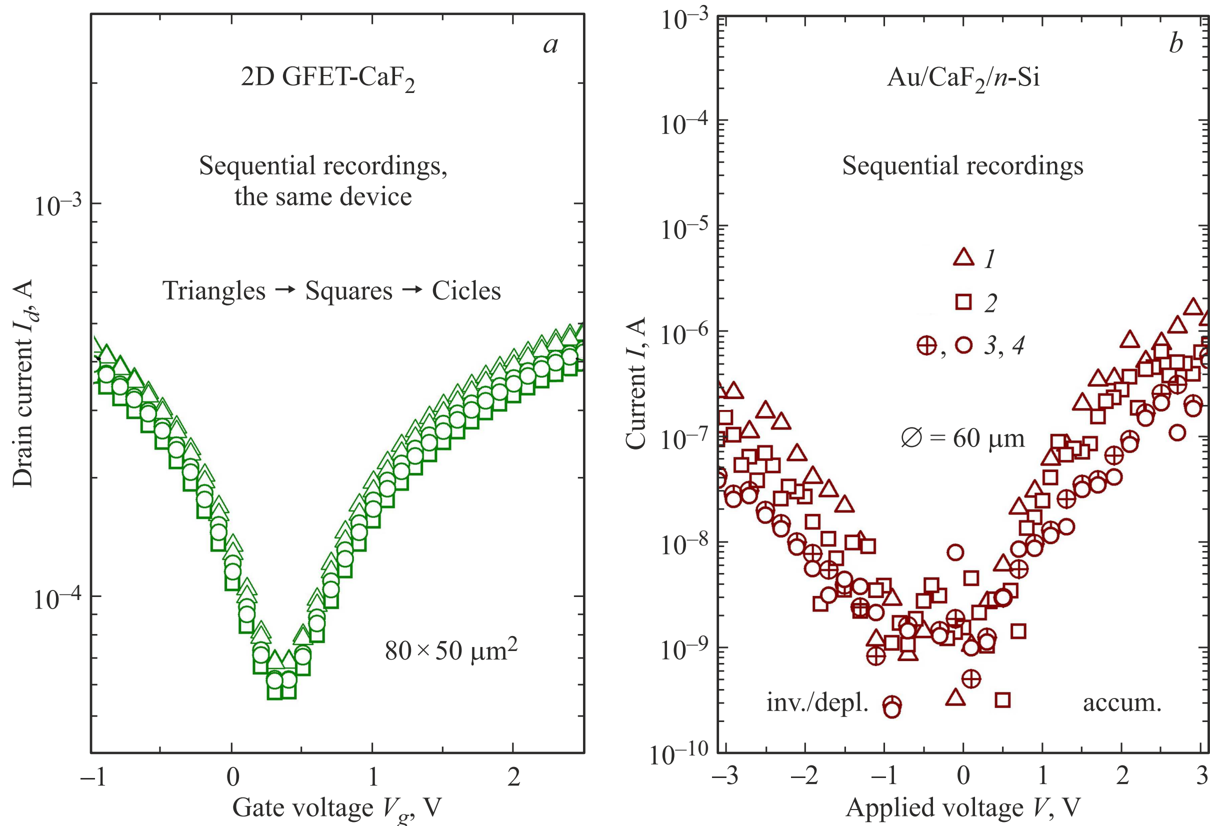

Figure 2. Performance reproducibility test. a — drain current I_d versus gate voltage V_g for 2D-GFET-CaF_2 at gate voltage $V_d = 0.3$ V, repeatedly registered on the same sample. b — repeatedly registered current-voltage curve of the controlled structure Au/CaF_2/Si.

obtained in specific processes (with nominally the same fluoride thickness).

4. Repeatability of characteristics of GFET prototypes with CaF_2

It was checked that at repeated recording the characteristics are reproduced with an accuracy of up to 10−20% for current (Figure 2, a). This proves the technology reliability in whole.

In the context of repeatability, it is interesting to highlight the role of fluoride. For this purpose, instead of graphene depositing on CaF_2 film, the gold electrodes were deposited through a mask, and after that the characteristics of the diode structure Au/CaF_2/n-Si were measured. As it was found, the current-voltage curve is reproducible (Figure 2, b) with the remark that usually, during the first recordings, the currents „move" a little down, decreasing by about half an order, after which reproducibility becomes almost ideal.

Summing up, it can be stated that there are no serious problems regarding the repeatability of characteristics during repeated measurements in the presented voltage ranges. No structures durability under overload conditions has been tested so far. The sample-to-sample spread of the characteristics will be discussed below.

5. Spread of the drain current values in transistor structures with CaF_2

The most simple parameter whose spread values are interesting to observe is current I_d at a given source-drain voltage V_d and some selected V_g (Figure 3). For definiteness it was assumed $V_d = 0.3$ V and $V_g = 2.0$ V.

Figure 3 shows histograms of current I_d. Average value $\langle I_d \rangle$ in the main Figure was 170 μA, standard deviation σ_{I_d} was 70 μA. A group of samples with almost identical characteristics is distinguished (separate histogram for it is given in the inset window 3, where $\langle I_d \rangle = 240$, $\sigma_{I_d} = 24\,\mu$A). The fraction of devices with characteristics included in this group was about quarter of all studied devices.

Figure 3 shows a diagram plotted for samples $80 \times 50\,\mu m^2$ in size, for other $L \times W$ the pattern is similar. It was natural to expect that an increase in the area would lead to an increase in the spread, since the larger the size, the more likely the presence of gross defects of various nature. However, it turned out that factor $\sigma_{I_d}/\langle I_d \rangle$, if it increases with the area of the channel, rises insignificantly, and in some cases it was more pronounced just for structures of the smallest area (specific results concerning the effect of size, for a slightly different indicator, will be presented in the next section).

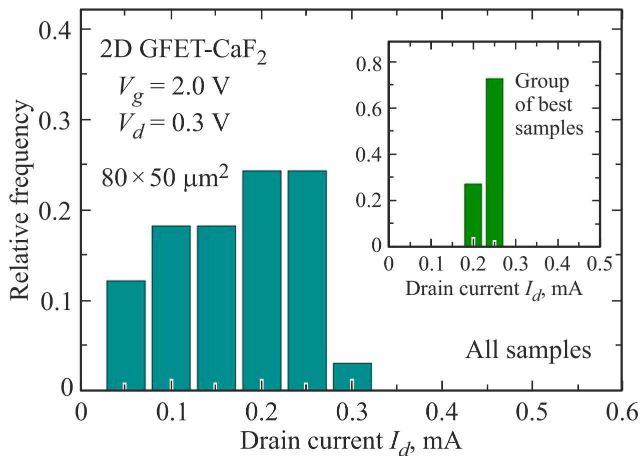

Figure 3. Histogram of the drain current I_d for 2D-GFET-CaF_2 device series at the drain voltage of $V_d = 0.3$ V and gate voltage of $V_g = 2.0$ V. The inset illustrates the same histogram for the group of „best“ devices, the spread of values there is less than in the main Figure.

The reason may be that graphene films grown by chemical deposition from the gas phase usually have a granular structure [8]. At the same time, the characteristic grain size (on average ~ 50 micron in our case) can vary across the film, which leads to a different number of grain boundaries inside the channels for different devices and, accordingly, a spread in characteristics. If we compare only small samples in terms of area, then there is one grain per sample. If we take large samples, then they will involve several grains, and with a sufficiently large number of them, effective averaging will result. Actually, we deal with different ratios between the linear size of the coverage area (size of the device) and the correlation length of fluctuations (linear grain size). A similar situation occurred when considering the spread of current passing through a dielectric with fluctuating local thickness at small and large sizes of electrode [9].

This does not negate the simplest above-mentioned assumption about the increase in defects probability with the area growth, i. e. different situations are possible.

6. Spread in position of drain-gate characteristic minimum

The drain-gate curves of the studied transistor structures $I_d(V_g)$ always have a minimum (see, for example, Figure 2, *a*). The operation mode consistent with the structure minimal conductivity is called a charge neutrality point (CNP). Sometimes this point is also called Dirac point [10], which is somewhat incorrect because „Dirac point“ — is a concept not from the circuit sphere, but from the analysis of dispersion relations for electrons states in a material.

Because the charge neutrality point (CNP) is crucial in structures with graphene, it is worth to monitor the spread of position of point V_g(CNP), I_d(CNP) from sample to sample. The corresponding data is given in Figure 4, separate for three dimensions. We see that the spread of parameter V_g(CNP) noticeably decreases as the structure size grows (horizontal width of the panel is different for different $L \times W$): while for the smallest structures the data for all devices lies in the range $0 \ldots 4$ V, for the largest structures the range is limited at $V_g(\mathrm{CNP}) \sim 1.2$ V. For the drain current in the charge neutrality point I_d(CNP), in contrast to V_g(CNP), this trend is less evident directly from the Figure; according to the calculations, $\sigma_{I_d(\mathrm{CNP})}/\langle I_d(\mathrm{CNP})\rangle$ makes 0.27 for the left and middle panels, and 0.33 for the right panel. I. e. no any serious worsening of the situation with spread value is observed when going from minimal to maximal area (while area changes in ~ 150 times).

There's no sense to bring the currents for different $L \times W$ to some common artificial „normalization“ — neither when discussing CNP-point, nor relative to the earlier described currents values I_d at a given V_d. The matter is that, the „operating cross-section“ here is not the area of the current-conducting layer, but its width W multiplied by graphene layer thickness, so that fixation of one and the same V_g for structures with different sizes L inherently leads to some non-equivalence of the modes.

7. Additional discussion

It is interesting to compare the „statistical“ results for GFET-CaF_2 with results for equivalent devices with other dielectric materials. We selected aluminum oxide Al_2O_3 (36 nm) as a pair for comparison. Some number of transistors were fabricated with this more „traditional“ insulating material compared to CaF_2. Histogram of current I_d at selected V_g, V_d (logically equivalent to „fluoride“ Figure 3) and „map“ of the charge neutrality point positions (equivalent to Figure 4 for CaF_2) for the group of devices are given in Figure 5, while the characteristics in terms of

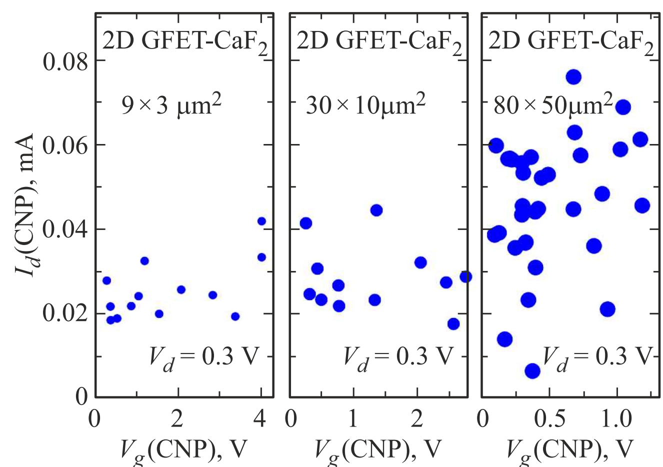

Figure 4. Positions of the charge neutrality point (in terms of voltage V_g, current I_d) for series 2D-GFET-CaF_2 with different sizes of the conducting channel.

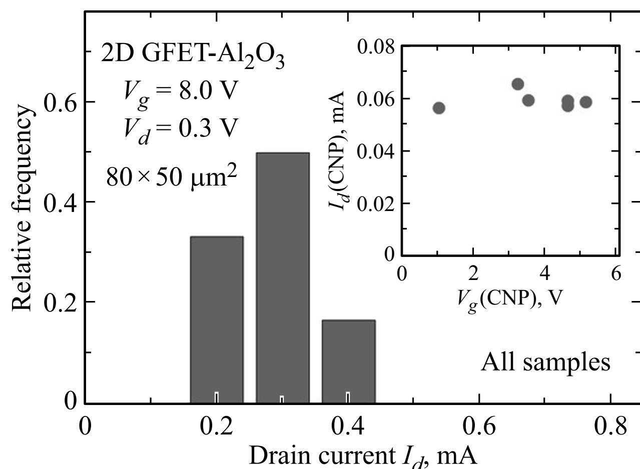

Figure 5. Positions of CNP-point (in terms of voltage V_g, current I_d) for 2D-GFET device series with aluminum oxide.

quality corresponds to the values in Figure 1. It can be said that in case of new dielectric CaF_2 the spread parameters were not worse (cf. Figures 3, 4) than in Figure 5, at that, the variations of voltage V_g (CNP), for example, in structures with aluminum oxide are even more distinct compared to the fluoride structures.

If we consider calcium fluoride structures without comparison with other materials, just by itself, then the spread can be assessed as satisfactory at this stage, especially since no steps have been taken to optimize the technology so far. It shall be especially stressed that in the „best" group of devices GFET-CaF_2 the spread of current values doesn't exceed two-three times, which is not bad.

Satisfactory spread values are important not only for 2D transistors, but also for — at least implicitly — other types of devices with CaF_2. From literature we know that in different times there was an issue of using CaF_2 in simple architecture FETs based on silicon, diamond and gallium arsenide [11,12]. In a large number of papers the prospects of using this material in the resonant tunneling diodes and super-lattices (along with Si or CdF_2) [13,14] was discussed. The first optimistic results in terms of stability and device-to-device data spread allow us to hope for successful use of the fluorides also in other applications, different from GFET-CaF_2.

8. Conclusion

In this paper, the situation with the spread of characteristics of our heterostructures, which are prototypes of field-effect transistors, with a two-dimensional graphene channel and calcium fluoride as a dielectric, was analyzed. This makes a significant addition to our previous studies of the functionality of such structures. The studied combination of materials „graphene and CaF_2" in this sphere is used practically for the first time; MoS_2 instead of graphene, or oxide dielectrics (like SiO_2, Al_2O_3) or hBN for isolator were used earlier.

The spread of characteristics should be considered acceptable at this stage, given that we are talking about the very first stage of research. The spreads from device to device were obtained, namely, for the values of the drain current I_d at fixed gate and drain voltages, as well as for the parameters of the charge neutrality point. As for reproducibility (repeatability of transistor curves with multiple recordings), no significant problems have been identified.

The studies performed are an important step on the way from proving the physical functionality of 2D GFET-CaF_2 to manufacturing the configuration-specific devices using this combination of materials. With regard to calcium fluoride, the results of the study indicate an acceptable level of technology at this stage, which is significant not only for the studied transistor structures, but also for other devices where this crystalline material is used. Further improvements may be associated with a decrease in the degree of heterogeneity of the fluoride thickness distribution over the area, as well as with the use of solid solutions of fluorides such as $Ca_{1-x}Mg_xF_2$.

Funding

The authors gratefully acknowledge financial support from the Russian Foundation for Basic Research (grant 21-52-14007 ANF_a).

Conflict of interest

The authors declare that they have no conflict of interest.

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Translated by T.Zorina