Semiconductors, 2023, Vol. 57, No. 4

Influence of single radiation defect cluster formation on transistor memory cell switching

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Received May 5, 2023
Revised June 29, 2023
Accepted July 6, 2023

The effect of a single radiation defects cluster formation on the transistor memory cell switching was studied. Estimates of the nuclear particle energy, capable of forming a cluster of radiation defects, causing a soft error of modern silicon transistors with various channel sizes. The failure cross sections for six and eight-element transistor memory cells are calculated for various technological processes under the influence of a neutron flux.

Keywords: transistor memory cell, radiation defect cluster, single event upset.

DOI: 10.61011/SC.2023.04.56424.15k

1. Introduction

Owing to its lower power consumption, which is attributable to the weakness of current flowing through a transistor channel in the off state, static random-access memory (SRAM) is used widely as small-size random-access or cache memory of microprocessors and programmable integrated logic circuits. The most efficient way to cut down the power consumption of a cell is to reduce the supply voltage. However, a reduction in supply voltage coupled with the miniaturization of transistors translate into a lower stability of the memory cell state, since the influence of noise and external interferences becomes more significant [1].

A memory cell may switch erroneously under the influence of single nuclear particles (SNPs); in certain cases, these SNPs cause irreversible faults and an inability to preserve the current state of a memory cell (the so-called „latchup"). The tolerance of a static memory cell to single event upsets (SEUs) is characterized by the ratio between the charge in the transistor channel causing switching of a static memory cell (critical charge) and the charge of radiation-induced carriers in the part of an SNP track passing through the sensitive region of the transistor (collected charge) [2]. If the critical charge is smaller than the collected one, switching and a SEU caused by it occur; in the contrary case, no switching (and, consequently, no SEU) is observed.

A static memory cell fault is induced by the formation of stable clusters of radiation defects, which act as scattering centers for mobile carriers, in the sensitive region of the transistor structure channel. If the channel conductivity in the on state drops below the critical value, a transistor enters a permanent non-conducting mode, thus causing an irreversible fault of a transistor memory cell.

The present study is made relevant by the fact that the critical charge and concentration of radiation defects causing SEUs and faults decrease as transistors become smaller, thus making a static memory cell less resistant to the influence of SNPs [3].

A number of papers focused on the simulation of SEU tolerance of static memory cells fabricated in accordance with modern semiconductor processes and subjected to irradiation have been published recently. The influence of cosmic radiation on a static memory cell based on 65 nm CMOS transistors was examined via numerical modeling in [4,5]. The response of a 22 nm memory cell to the influence of heavy nuclear particles (HNPs) was modeled in [6]. Radiation-induced defects were taken into account in the modeling of ionization current in a charged particle track in [7].

The emergence of SEUs in integrated circuits under the influence of neutrons has first been predicted theoretically in [8] and verified experimentally in [9] for 3-μm bulk-silicon dynamic memory elements.

The „silicon-on-insulator" (SOI) technology allows for a considerable enhancement of SEU and fault tolerance of components of integrated circuits under irradiation [3]. Experimental studies of the SEU tolerance of 350 nm SOI static memory performed in [10] revealed the presence of SEUs under irradiation with fast neutrons.

The SEU mechanism common to all the mentioned studies is as follows: SNPs enter a memory cell transistor in the off state, transient ionization processes induce its unwanted transition to the on state, and memory cell switching is observed as a result. Another SEU mechanism for a static memory cell has been proposed for the first time in [11]. Instead of the production of inequilibrium charge carriers, which has been examined in detail for transistors fabricated following modern semiconductor processes [4–6], this mechanism associates SEUs with the process of formation of a disordered region. When a cluster of radiation defects forms in the channel of a transistor, its conductivity may fall below the critical value, which sets the boundary between on and off states, due to additional scattering of mobile carriers off the produces radiation defects. If the time period of conductivity reduction is sufficiently long, abnormal switching of a memory cell occurs. As a cluster stabilizes due to the recombination of closely spaced Frenkel pairs, the channel conductivity returns to its initial level sufficient for normal transistor operation; therefore, a failure observed in this case is reversible. The discussed SEU mechanism is relevant only if the cell switching time is comparable to the time of formation of a disordered region. This condition may be satisfied in memory cells consisting of modern transistors with a minimum feature size below 20 nm.

This scenario of short-term radiation-induced reduction in the transistor channel conductivity falls in between a reversible failure due to a temporary increase in the transistor channel conductivity owing to ionization effects and an irreversible fault of a memory cell element as a result of long-term channel conductivity reduction due to structural damage caused by SNPs. The present study is focused on analyzing the influence of formation of a radiation defect cluster on the SEU tolerance of modern transistor memory cells.

2. Objects under study

Six- and eight-element memory cells based on transistors with minimum feature sizes of 20 and 7 nm were chosen for analysis. A classical static memory cell consists of six transistors: four of them form two invertors with positive feedback, and another two transistors are used for read and write operations. Additional transistors in an eight-element memory cell form a read buffer that is needed to separate read and write operations [12].

The geometric dimensions of the working region of modern transistors in a static memory cell are listed in Table 1 [13].

Table 1. Geometric dimensions of the working region of modern transistors [13]

Dimension	Semiconductor process	
	20 nm	7 nm
Gate length, nm	24	11
Gate height, nm	28	18
Gate thickness, nm	15	7

Two groups of static transistor memory cells operating in the high-performance (HP) mode with a low threshold voltage and in the low power consumption (LP) mode with a high threshold voltage are distinguished on the basis of the threshold voltage level at which transistor switching occurs. The supply voltage of all transistors examined in the present study varies within the range of 0.7−0.9 V. The threshold voltage for the low power consumption mode is 0.4 V at a supply voltage of 0.5 V. The write time is defined as the time interval between the emergence of a control signal in the write line and switching of the cell state. The state write times in 6T- and 8T-SRAM cells in the HP mode are listed in Table 2 [13].

Table 2. Write times of static memory cells [13]

Static memory cell	Write time, ps	
	20 nm	7 nm
6T	7.5	2.5
8T	9	3

The hold static noise margin (HSNM) for the studied memory cells is ~ 200 mV [13]. If the noise amplitude is > 200 mV, a cell changes its state to an opposite stable one. The ratio of currents in on and off states, which was calculated with the use of current–voltage curves of the examined transistors and with HSNM taken into account, is 0.3.

Thus, a SEU occurs in the event of formation of radiation defect clusters (RDCs) if the current of one of the transistors in the on state drops to off-state levels and remains there for an interval of time exceeding the state write time of a memory cell.

3. Mathematical model

One needs to know the energy distribution of neutrons in order to calculate the number of SEUs per a static transistor memory cell and induced by the RDC formation under neutron irradiation. A prompt fission spectrum is considered in the present study. It is continuous and extends from several kiloelectronvolts to 18 MeV with an average energy of ~ 2 MeV. A number of empirical formulae characterizing the fission spectra of particular nuclei are currently available. Kranberg [14] has proposed the following formula that is based on experimental measurements and characterizes the energy distribution function of ^{235}U fission neutrons:

$$\phi(E_n) = 0.453\left[\mathrm{sh}(2.29E_n)^{0.5}\right]\exp\left(\frac{-E_n}{0.965}\right), \qquad (1)$$

where E_n is the neutron energy.

At a given flux, the probability of penetration of a neutron into the channel of a transistor and interaction with lattice atoms may be estimated as [15]

$$P = 1 - \exp(-\sigma F_n V N_{\mathrm{at}}), \qquad (2)$$

where σ is the neutron scattering cross section in the given energy range, F_n is the integral neutron flux in the given energy range, V is the volume of the working region of

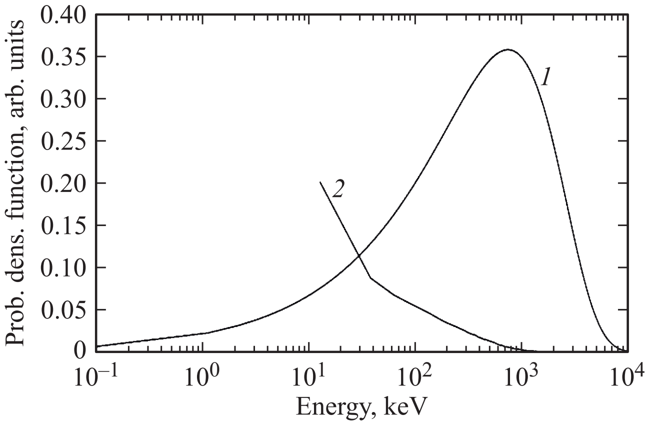

Figure 1. Probability density functions for the energy distribution of particles: *1* — fast neutrons of a prompt fission spectrum; *2* — primary recoil atoms.

a transistor, N_{at} is the concentration of matter atoms, and P is the probability of interaction of a neutron with a lattice atom.

The energy of each neutron interacting with matter atoms needs to be calculated in accordance with distribution function (1). Energy E_A of a primary recoil atom of silicon is then determined in accordance with the model of interaction of elastic spheres [16]:

$$E_A = \frac{4A}{(1+A)^2} E_n \sin^2\left(\frac{\vartheta}{2}\right), \tag{3}$$

where ϑ is the recoil angle between the directions of neutron motion before and after a collision and A is the atomic weight. In the case of isotropic neutron scattering, all recoil angles ϑ within the range from 0 to 2π are equally probable.

Figure 1 presents the spectra of neutrons and primary recoil atoms calculated with the use of relations (1) and (3). The neutron spectrum is bounded by an energy on the order of tens of megaelectronvolts with an average value of ~ 2 MeV. The spectrum of primary recoil atoms of silicon is bounded by an energy of several megaelectronvolts with an average value of ~ 250 keV.

If the energy of a recoil atom falls within the range from $E_1^{(\text{kp})}$ to $E_2^{(\text{kp})}$, a SEU of a static transistor memory cell induced by the process of formation of a single radiation defect cluster is observed. Primary recoil atom energy $E_1^{(\text{kp})}$ corresponds to the case when the process of RDC formation causes abnormal switching of a memory cell. Primary recoil atom energy $E_2^{(\text{kp})}$ corresponds to the case when the process of RDC formation causes a memory cell fault. The overall number of SEUs calculated this way for each neutron among N_{act} characterizes the SEU cross section of a memory cell.

In order to determine the values from $E_1^{(\text{kp})}$ to $E_2^{(\text{kp})}$ for each of the considered semiconductor processes, one needs to calculate the variation of the transistor current under zero gate bias at the moment of RDC formation. An original approach relying on the self-consistent Monte Carlo method [17], where the mechanism of scattering off a forming radiation defect cluster is considered in addition to other factors, was used for the purpose. An RDC may be considered electrically neutral on the examined time scales of several picoseconds, since the process of capture of mobile carriers to deep energy levels of radiation defects in silicon takes several microseconds [18]. Rate λ_{form} of scattering off a forming neutral RDC then depends on the concentration of point defects that varies in time due to the processes of thermal expansion and stabilization of an RDC. In a manner similar to the scattering off neutral impurity atoms [19], the rate of scattering off a forming RDC may be expressed as

$$\lambda_{\text{form}}(t) = 20\,\frac{N_{\text{def}}(t)}{V_{\text{ch}}}\,\frac{\varepsilon\varepsilon_0 h^2}{(m^* q)^2}, \tag{4}$$

where h is the Planck constant, N_{def} is the number of Frenkel pairs, ε is the permittivity of the material, ε_0 is the permittivity of vacuum, m^* is the effective mass of carriers, and q is the electron charge. The condition of stationarity of the process of defect formation with respect to mean carrier free time τ is an important condition of applicability of this approach:

$$\tau \ll \frac{1}{\lambda_{\text{form}}(t)}. \tag{5}$$

It should also be noted that the rate and the angle of scattering off a forming RDC are independent of carrier energy.

In the present study, LAMMPS [20] was used to model the dynamics of RDC formation and accompanying ionization processes. This software implements the method of classical molecular dynamics coupled with the two-temperature model of the atomic and electronic lattice subsystems [21]. The following parameters are estimated at each time point: number of Frenkel pairs N_{def}, the energy transferred to the electronic subsystem; and the temperature of electron–hole plasma.

The time interval within which the drain current corresponds to the off state of a transistor is estimated based on the obtained temporal dependences of the transistor drain current. If this time interval exceeds the characteristic switching time of a memory cell, a SEU occurs. The energy of a primary recoil atom inducing a SEU of a memory cell corresponds to $E_1^{(\text{kp})}$. If the transistor drain current is not restored within an interval of time being an order of magnitude greater than the switching time, a SEU evolves into a memory cell fault. The energy of a primary recoil atom inducing a memory cell fault corresponds to $E_2^{(\text{kp})}$. Note that the influence of parasitic inductances and capacitances of interelectrode connections in a memory cell is neglected in the presented model.

4. Calculation results and discussion

Figure 2 shows the temporal dependences of relative variation of the transistor drain current at the moment of formation of a cluster of radiation defects induced by primary recoil atoms with various energies in the channel of a 7 nm transistor.

Figure 3 presents the temporal dependences of relative variation of the transistor drain current at the moment of formation of a cluster of radiation defects induced by primary recoil atoms with various energies in the channel of a 20 nm transistor. Comparing the data in Figs. 2 and 3, one finds that a transistor with a larger minimum feature size switches to the off state at higher energies.

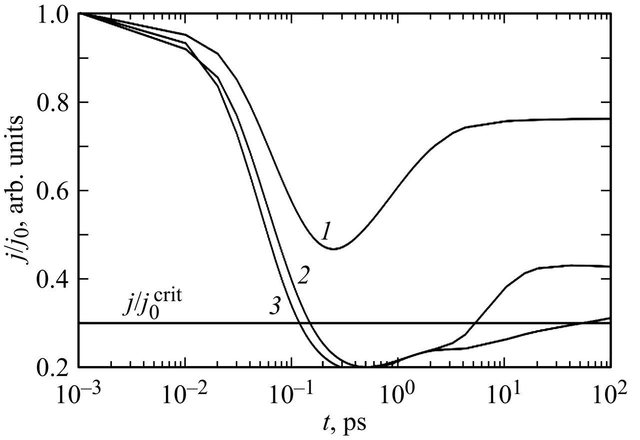

Figure 2. Temporal dependences of relative variation j/j_0 of the drain current of a 7 nm transistor in the process of formation of a cluster of radiation defects induced by primary recoil atoms with the following energy [keV]: *1* — 12, *2* — 30, and *3* — 50. Critical ratio $j/j_0^{\rm crit}$ at which the transistor switches to the off state is also shown.

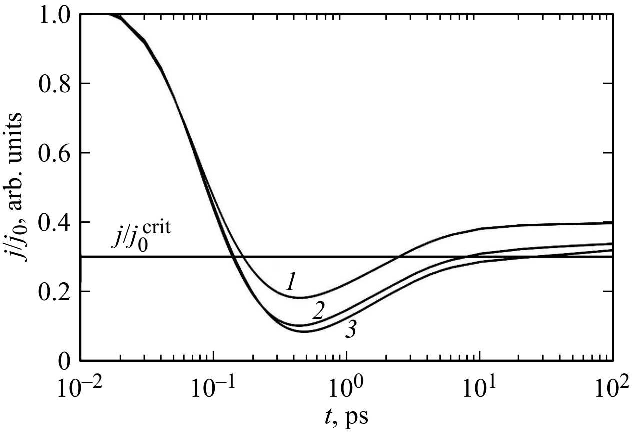

Figure 3. Temporal dependences of relative variation j/j_0 of the drain current of a 20 nm transistor in the process of formation of a cluster of radiation defects induced by primary recoil atoms with the following energy [keV]: *1* — 50, *2* — 100, and *3* — 130. Critical ratio $j/j_0^{\rm crit}$ at which the transistor switches to the off state is also shown.

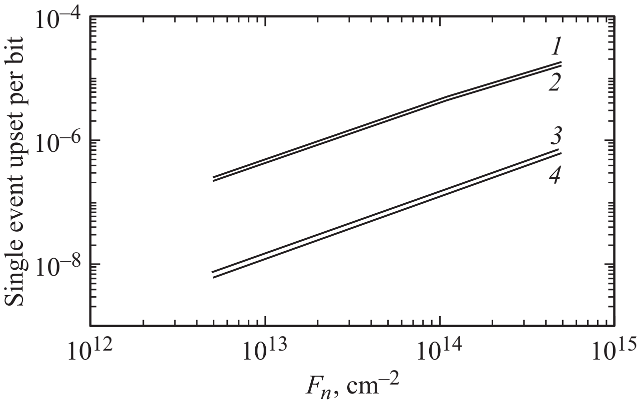

Figure 4. Dependences of the number of SEUs per bit induced by the RDC formation process on the integral neutron flux for 6T- and 8T-SRAM cells based on 20 nm and 7 nm transistors: *1* — 8T-20 nm, *2* — 6T-20 nm, *3* — 8T-7 nm, and *4* — 6T-7 nm.

The variation of drain current at the moment of RDC formation induced by a primary recoil atom with an energy in the range of 3–200 keV in the transistor channel was modeled for semiconductor processes listed in Table 1, and the values of $E_1^{\rm (kp)}$ and $E_2^{\rm (kp)}$ were calculated. The calculation results are presented in Table 3. A SEU occurs as a result of RDC formation in memory cells at primary recoil atom energies falling within the ranges of 100–200 keV and 30–40 keV in the case of 20 nm and 7 nm transistors, respectively.

These energy ranges were used to calculate the per-bit number of SEUs induced by the process of RDC formation in a memory cell at various integral neutron fluxes. The obtained data are presented in Fig. 4. The per-bit cross

Table 3. Primary recoil atom energies at which the process of RDC formation induces a SEU ($E_1^{\rm (kp)}$) and a fault ($E_2^{\rm (kp)}$) of a transistor memory cell

Static memory cell	$E_1^{\rm (kp)}/E_2^{\rm (kp)}$, keV	
	20 nm	7 nm
6T	99/191.4	28.9/38.88
8T	101.4/211.7	29.15/41.2

Table 4. Per-bit cross sections of SEUs caused by the RDC formation process

Static memory cell	SEU cross section per bit, cm^2/bit
6T-7 nm	$1.23 \cdot 10^{-21}$
8T-7 nm	$1.46 \cdot 10^{-21}$
6T-20 nm	$3.2 \cdot 10^{-20}$
8T-20 nm	$3.65 \cdot 10^{-20}$
6T-350 nm [17]	$1.4 \cdot 10^{-17}$

sections of SEUs caused by the RDC formation process were also derived from these dependences (see Table 4). The experimental total SEU cross section per bit determined for the 350 nm semiconductor process [17] is shown in Table 4 for comparison. The calculated SEU cross sections for irradiating neutrons of a prompt fission spectrum, six- and eight-element transistor memory cells, and different semiconductor processes are several orders of magnitude lower than the values observed experimentally. This is attributable to the fact that the experimental cross section represents SEUs induced by ionization processes instead of the RDC formation process. However, the obtained estimates suggest that the RDC formation process should exert a more and more significant effect on the total number of SEUs as the minimum feature size of transistors decreases.

5. Conclusion

The influence of formation of a single radiation defect cluster on the transistor memory cell switching was examined. According to the obtained estimates, a radiation defect cluster causing a SEU of modern silicon transistors is produced by a primary recoil atom with its energy falling within the range from tens of kiloelectronvolts to several hundred kiloelectronvolts. These estimates provide an opportunity to predict more accurately the total number of SEUs of modern static memory cells under irradiation.

Funding

This study was carried out under the scientific program of the National Center for Physics and Mathematics („Nuclear and Radiation Physics“ project).

Conflict of interest

The authors declare that they have no conflict of interest.

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Translated by D.Safin