Device Performance Optimization of Organic Thin-Film Transistors at Short-Channel Lengths Using Vertical Channel Engineering Techniques

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This paper presents a finite-element-based two-dimensional numerical simulation study of the vertical channel engineering approaches for controlling the short-channel effects (SCEs) in organic transistors based on thin-film transistor technology (OTFTs). The impact of gate-oxide thickness T_{Ox} scaling and usage of high-permittivity gate dielectric material has been analyzed for a bottom-contact organic thin-film transistors at channel length of $0.7\,\mu$m. The techniques have been used to investigate the impact on drain-induced barrier lowering (DIBL), sub-threshold slope, and $I_{\mathrm{On}}/I_{\mathrm{Off}}$ ratio. The results have shown a significant reduction in values of DIBL and sub-threshold slope in short-channel OTFTs when either of the channel engineering techniques are employed. A high $I_{\mathrm{On}}/I_{\mathrm{Off}}$ ratio of the order of $\sim 10^7$ has been achieved using a high-permittivity gate-oxide material. It has been observed that using a high-permittivity gate dielectric material, apeak value of $I_{\mathrm{On}}/I_{\mathrm{Off}}$ ratio can be achieved for an equivalent oxide thickness of 5 nm. The results suggest that the desirable transistor performance can be achieved through proper selection of gate-oxide material and thickness.

Keywords: DIBL, high-κ gate dielectric, leakage currents, sub-threshold.

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