Patterning approach for detecting defect in device manufacturing

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Compact handheld devices which were a dream in the past are now a reality; this has been enabled by miniaturization of circuit architectures including power devices. Scaling down of the design feature sizes does come with a price with an increase in systematic defects during chip manufacturing. There are generally two methods of inline defect detection adopted to monitor the semiconductor device fabrication — optical inspection and electron beam inspection. The optical inspection uses ultra-violet and deep ultra-violet (UV/DUV) light to find patterning defects on the wafer. While the electron- beam inspection uses electron charge and discharge measurement to find electrical connection defects, both are a costly procedure in terms of resources and time. The physical limit of feature resolution of the optical source is now making the defect inspection job difficult in miniaturized application specific integrated circuit (ASIC). This study is designed to test the patterning optimization approach on both inspection platforms. Using hotspot analysis weak locations are identified in the full chip design, and then they are verified in the inline wafer inspection. The criterion for hot-spot determination is also discussed in this paper.

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1. Introduction

There are several sources that contribute to defect generation during IC manufacturing cycle from design to fabrication. It is shown that co-optimization of thermal and electrical objective results in a floor plan that is attractive from both perspectives [1]. Design optimization based on the enumeration of process corners has been widely used, but still cannot guarantee robust design for manufacturing [2]. It has been shown that using optimization with the ellipsoidal uncertainty approach, robust design can be obtained with guaranteed yield bound and lower design cost, and most importantly, the problem size grows linearly with number of uncertain parameters [3]. The fabrication processes have not changed much since 45 nm technology node. The traditional approach (as shown in Fig. 1) has been that after the design tape out the responsibility of the semiconductor device yield is owned by the fabrication facility. When a layout — the geometrical shapes that collectively describe a circuit — adheres to all design rules, the fabricated circuit functions according to the design [4,5]. With the demand for accommodating more and more functions in one chip the complexity of design has increased over the years [6,7]. Along with reducing the feature size on the wafer, it's becoming hard for the fabrication processes to handle marginalities. It is becoming increasingly difficult to design and manufacture the most complex systems-on-a-chip (SOC) without a unified approach which allows taking into account the relationship between the package and the integrated circuits (IC) design flows [8]. This has necessitated close working relationship between circuit designers and fab process owners and has given birth to new steps in the manufacturing cycle — i) Inclusion of more manufacturing marginalities in design qualification (DRC — Design rule Check), ii) Modelling the target manufacturing process to simulate and verify the design before committing to mask. Several OPC (Optical Proximity Correction) techniques are employed to modify the design patterns to enhance their resilience to the fabrication processes [9–12].

Despite of all these additional checks still process marginalities are observed on the wafer around certain design feature types [13,14]. Now there is a need to integrate learning from the design into the fabrication processes. In this paper design based methodology has been successfully attempted on a 28 nm design to find

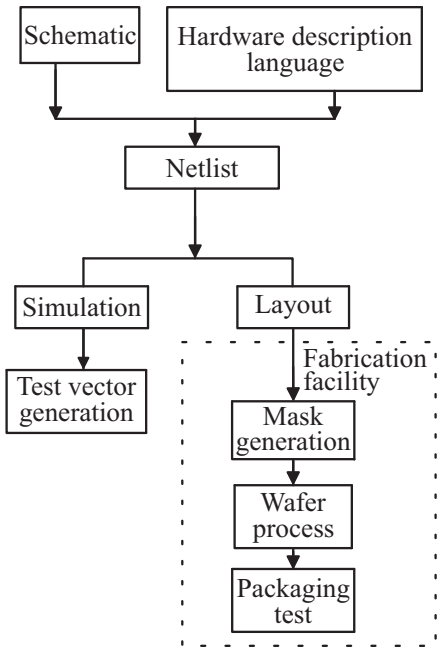

Figure 1. Traditional approach of IC fabrication cycle.

pattern defects during fabrication. The idea is to understand design marginalities that cause systematic failures during fabrication. This proves to be a valuable input to optimize certain process recipes to handle such marginalities and make the manufacturing line more robust. The physical limit of feature resolution of the optical source is now making the defect inspection job difficult in miniaturized ASIC. The cycle time and the defect count in performing full chip wafer inspection with high sensitivity settings are not affordable.

2. Pattern induced defects on wafer

The target design goes through a series of transformations to ensure the system design goals are met for any power electronics device — like area, time delay, power dissipation, current density, etc. These transformations are supposed to make the design robust to handle fab processes — like Lithography, Etch, Chemical Mechanical Planarization (CMP), etc. At sub 45 nm design rule accurately modelling all the fab processes is not straightforward [15]. This challenge makes certain design structures prone to generate defects under a given set of fab process [16]. Fig. 2 shows the changes occurring to the layout during Photolithography process. These changes in the layout can cause connection, reliability and other chip failures [17].

Various resolution enhancement techniques, like proximity corrections, are adopted to improve pattern fidelity on silicon and prevent such failures. Despite such efforts the interaction design with various fabrication processes has shown marginalities on wafer generating defects [18]. The design structures which are prone to defects, in spite of all known corrections, can be deduced by studying the frequent failures on the wafer after major fabrication processes.

Generally, it is found that certain combinations of pattern shape and size can render the structure weak on the wafer. For example, some special topological structures in the chip layout may result in leakage in Complementary Metal Oxide Semiconductor (CMOS) devices due to the micro loading effect [19]. Similarly, it has been shown that layout attributes like layout density and feature perimeter sum can be used

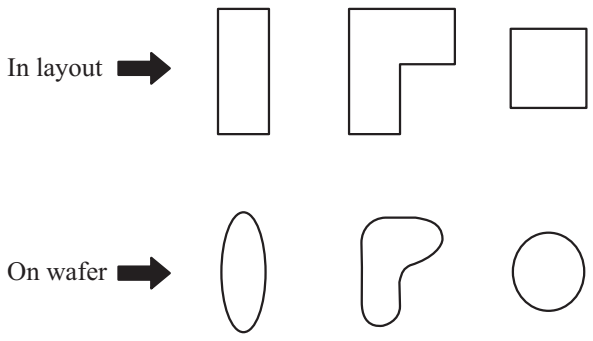

Figure 2. Layout to silicon transformation-degradation in pattern fidelity.

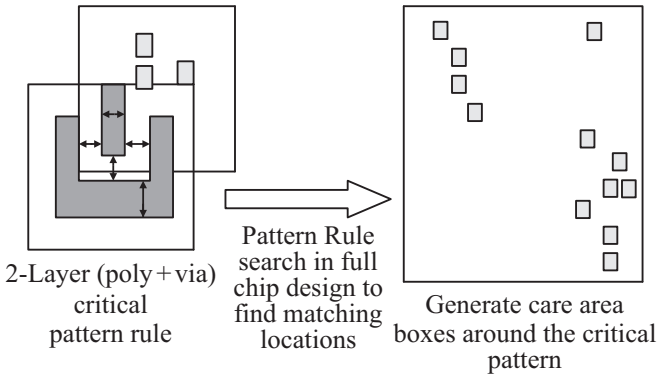

Figure 3. Critical pattern definition and generation of scan region.

to compute the post-electroplating topography, modelling the array height and the step height simultaneously [20]. Such knowledge helps to define pattern rules for full chip layout analysis to search the hot-spots. After wafer inspection, the defect map generally contains thousands of defect points on wafer map that contains both random and systematic defects as well as false defects depending on wafer condition and inspection settings. It is hard to point out which of them are systematic and caused by pattern failure instead of random defects like particle [21]. Similar design analysis approach helps in overlaying the defect map on layout and determining the most frequently failing pattern locations. Optical wafer inspection is done for physical defect detection, while *e*-beam wafer inspections will detect voltage contrast defects [22]; here the focus is on pattern related defects.

The analysis is done in two steps:

i. Pattern based care area generation.

ii. Pattern based binning and ranking of defects.

For performing any wafer inspection the region in a die need to be defined. This region of inspection is called „care area“ — it needs to be optimized for high sensitivity inspection to find small and critical defects on the wafer. If the care area is not optimized, then there are chances of wasting inspection time on detecting irrelevant defects that also hampers in post-inspection analysis. With the reduction of feature sizes on wafer it is now impossible to decipher them under optical microscope used for wafer inspection. In such a case layout design has been demonstrated to be useful to define the critical regions in the chip. Fig. 3 shows that the overlay of via and poly-silicon layers would be critical for chip yield and hence such locations in the full chip design has been searched and box generated, shown with yellow boxes, defining the care area for wafer inspection. In Fig. 3 the process layers polygons from poly-silicon and via are shown on left side; the rectangular boxes on the right side show the care areas where defect inspection must be done.

After the wafer optical inspection, the defect counts reported are typically in thousands rendering the defect

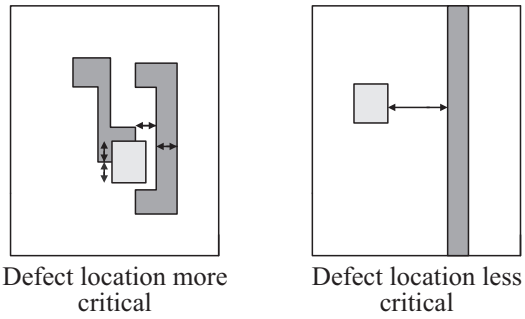

Figure 4. Pattern definition for defect binning and ranking.

analysis cumbersome process to find out the real systematic defects. This is like finding a small pin in a haystack. Fig. 4 shows design guided analysis approach where the defect file from the wafer inspection result is transformed into design coordinate locations and overlaid on the respective process layer layout. Then, the possibility of the defect is determined depending on its location with respect to layout features. The closer is the defect to small features or if it affects more than one feature, the more critical the defect will be. The process layer pattern proximity with the defect location is shown in Fig. 4.

3. Pattern definition for defect binning and ranking

The efficacy of the proposed methodology of pattern rule search for finding critical pattern hot- spots in the design, as compared to the traditional approach of full die scan was done. The pattern rule definition is outlined using the example shown in Fig. 5. The hotspots are from the defect database for any technology which encompasses defect capture from design building to wafer manufacture processes like lithography, deposition, etch, polish, etc.

The pattern rules are determined based on the pattern shape and its neighbourhood. The edge size limits are calculated by Design for Manufacturing (DFM) definitions.

Rule1: Distance edge-H to edge-$d < L_H$,

Rule2: Distance edge-A to edge-$c < L_A$,

Rule3: Distance edge-h to edge-$d < L_h$,

Rule4: Distance edge-G to edge-$A < L_G$,

Rule5: Distance edge-e to edge-$G < L_e$

Here the violation limits L_H, L_A, L_h, L_G, L_e are known from the DFM rule set. The benefit of this proposed approach is to be able to combine multiple 3D violations set in one place, thus reducing the time to determine critical defects in full chip.

The condition can be set for catching violation of any of the above rules as below:

```
Begin{
      if (Rule1=True || Rule2=True || Rule3=True
       || Rule4=True || Rule5=True)
      {function (generate care area)}
      else{return0}
      }
  End
```

Similar rules were defined to find pattern hotspots in the design, and then care area box is generated around these hotspot locations. This is fed into the inspection machine for full wafer scan. In order to accomplish defect ranking, the inspection result is first binned based on design background as below:

i. Defects falling exclusively in open Space or Dummy features => Bin0.

ii. Defects falling on patterns defined by critical rule definition => Bin1.

iii. Rest of area => Bin2.

It is to be noted that the optical inspection region extends beyond the critical patterns as a consequence of its stage shift. So even if the inspection care areas were defined by the design prodigality, an extended region beyond the critical pattern is inspected and defects are reporting from there as well (that will fall in Bin0 or Bin2). Based on the purpose of the scan different weights can be assigned to each Bin. For this study since we were focusing only on the efficacy of the critical design approach, these weights were assigned: Bin0 = 0, Bin1 = 1, Bin2 = 0.1. The goal was only to sample the defects from the regions that were originally intended to get inspected. Only 10% of the defects from Bin2 is sampled to cover for the stage shift induced overlay error. For line monitoring different set of weights for each of the bins would be advisable so as to cover all systematic and random defects that can fall in any

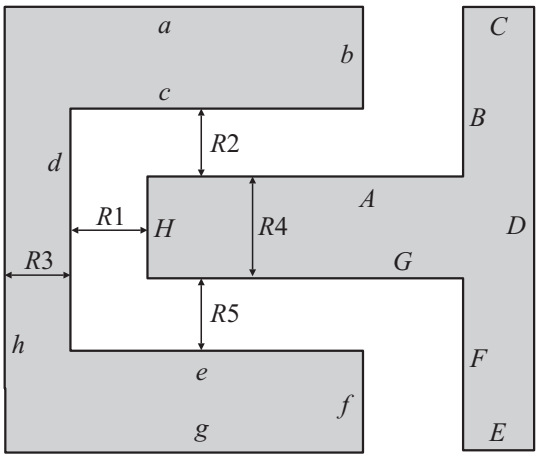

Figure 5. Pattern Rule definition.

of the bins. Further breakdown of rank is done with optical properties of the defect patch images from the inspection tool (intensity of defect signal). The exact name of the parameter is specific to the inspection tool platform used.

Fig. 6 shows the result table of the optical inspection — more types of patterning defects were found using the pattern rule definition than the traditional approach. It can be observed that random defects like Particle and Scratch are not predicted by the hot-spot approach — this is the limit and also the benefit of the pattern based analysis. One to one correlation of the hotspot prior to scan with the defect detection can be seen in Fig. 7. The same approach of weak point determination was applied to e-beam inspection. In this case, additional rule of checking overlay connections to the previous layer was also added to the pattern rule definition — this is to detect Voltage Contrast (VC) defects. This is the primary benefit of *e*-beam inspection — to be able to find connection fails to previous layers as contrast variation.

Depending on the voltage bias and other inspection settings the translation of Dark Voltage Contrast (DVC) and Bright Voltage Contrast (BVC) to open and short defect changes. In this case, the blocked contact to the source and drain of *p*-type Metal–Oxide Semiconductor (PMOS) transistor region caused DVC.

Defects	Full die scan	Hotspot scan
Voids	10	18
Breaks	1	6
Bridges	0	5
Scratch	9	0
Particles	5	0

Figure 6. Optical inspection result around design hot-spots.

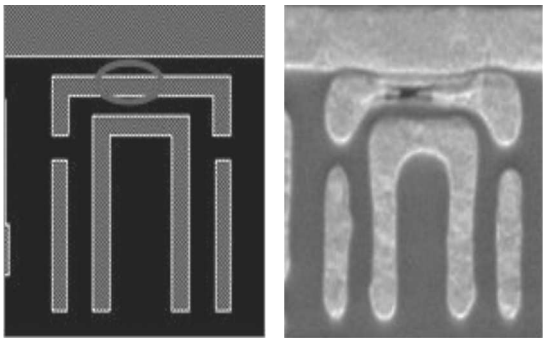

Figure 7. Design hot-spot to SEM image correlation.

Defects	Hotspot scan
Pattern bridging	10
DVC	5

Figure 8. Defect detection from *e*-beam inspection.

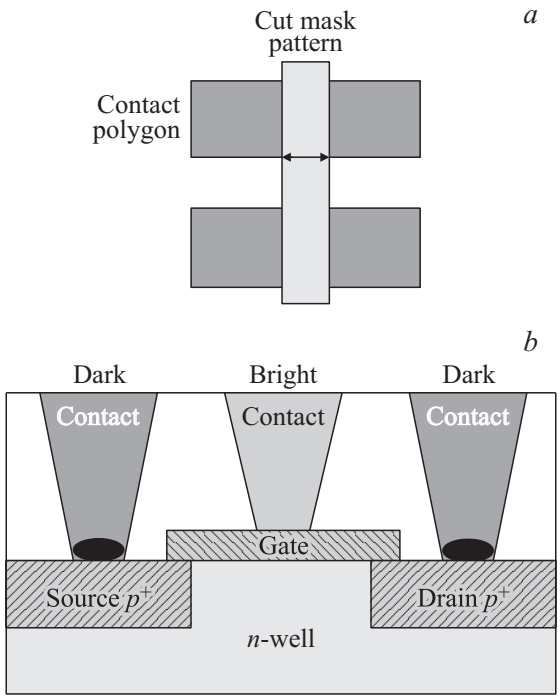

Figure 9. Defect Mechanisms: *a* — physical defect found in *e*-beam inspection; *b* — electrical defect found in *e*-beam inspection.

Fig. 8 shows the defect table that were trapped on full wafer *e*-beam inspection. The pattern bridging, was the consequence of the insufficient cut mask between two adjacent horizontal contact polygons. Depending on the voltage bias and other inspection settings, the translation of DVC and BVC to open and short defect, varies. In this case, the blocked contact to the source and drain of the PMOS transistor region causes DVC.

The defect mechanism is explained in Fig. 9. The physical defect (Fig. 9, *a*) of pattern bridging is a consequence of the shrink in the cut mask pattern. This is caused by the design/litho operation. On the other hand, the electrical blockage in the path of the contact for the source and the drain of PMOS transistor causes dark voltage contrast as shown in Fig. 9, *b*. This should otherwise be bright with the positive reference voltage.

4. Conclusions

In spite of all the checks at each step in the chip manufacturing the yield is always a challenge. Chip fabricators are always on the lookout for the novel techniques to reduce the yield loss. The methodology of weak point determination by using a pattern rule definition has been tested for both patterning defects and voltage contrast connection defects. The knowledge of the process fail

from design stage to manufacturing processing need to be accumulated and used as a learning pool for building the weak pattern rules. Optical and *e*-beam wafer inspection can be guided using the pattern analysis approach thus reducing the learning cycle for yield improvement. The determination of weak points based on DFM data base will optimize the care area for optical wafer inspection and also guide the *e*-beam inspection for the detection of connection defects. The dilemma — which defects to be filtered from wafer inspection result, is also solved by taking aid from pattern analysis. The overlay of physical defect location with the pattern process layer helps to determine the design critical locations. The defects lying on critical layout features will certainly affect the chip operation.

Moreover, the sensitivity setting of the wafer inspection will determine the type of defects that will be caught-line edge roughness and size shrink are considered nuisance defects if the size variation is not affecting any layout connection. Similarly wafer defect locations on dummy patterns or open spaces will also be a nuisance. Pattern based analysis will easily filter these nuisance defects making the whole procedure of defect analysis manageable, efficient and result oriented. Using this approach the manufacturing facility can find design/process marginalities that cause systematic defects. The correlation of this, pattern based approach shown in this paper with the traditional approach demonstrates the efficacy of the proposed method. The confirmation of detecting process critical defects on wafer further verifies the proposed approach. After confirmation of systematic fail on a wafer, a feedback loop can be created using this approach to improve the design/process such as to fix the marginalities for robust manufacturing. There will be different types of pattern rules that can be used to determine weak points in the design. For power electronics devices, it is imperative that any Critical Dimension (CD) variation of electrical lines may cause reliability issues, especially when miniaturization of the system is done. This is so because any system miniaturization does not scale down all the design parameters with the same scale. The design for manufactured approach is not only restricted to the chip manufacturing, but also has successful applications in other manufacturing industries [23,24]. Since the wafer inspection is performed in all key manufacturing steps, thus this proposed pattern based approach can be used iterative to correlate multi-layer defects and also learn defect propagation. This approach of finding pattern defects in miniaturized IC will help in determining and monitoring design weak points through the manufacturing cycle.

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